PY32F072-E Datasheet

32-bit ARM® Cortex®-M0+ Microcontroller

Puya Semiconductor (Shanghai) Co., Ltd.

PUYA

PY32F072-E Series

ARM® 32-bit Cortex®-M0+ Microcontroller

Features

- Core
  - ARM® 32-bit Cortex®-M0+ CPU
  - Frequency up to 72 MHz
- Memories
  - Maximum 128 KB Flash memory
  - Maximum 16 KB SRAM
- Clock management
  - 4/8/16/22.12/24 MHz High-speed internal RC oscillator (HSI)
  - 32.768 kHz Low-speed internal RC oscillator (LSI)
  - 4 to 32 MHz High-speed external crystal oscillator (HSE)
  - 32.768 kHz Low-speed external crystal oscillator (LSE)
  - PLL (supports 2/3 multiplication of HSI or HSE)
- Power management and reset
  - Operating voltage: 1.7 ~ 5.5 V
  - Low power modes : Sleep and Stop
  - Power-on/power- down reset (POR/PDR)
  - Brown-out reset (BOR)
  - Programmable voltage detector (PVD)
- General-purpose input and output (I/O)
  - Up to 58 I/Os, all available as external interrupts
- 7-channel DMA controller
- 1 x 12-bit ADC
  - Up to 16 external channels
  - Conversion range: 0 to V_{REF+}
- 2 x 12-bit DAC, supports 2 channels
- 3 x analog comparators
- 3-channel operational amplifier
- Support 8 * 36 / 4 * 40 LCD
- 13 timers
  - 1 x 16-bit advanced-control timer (TIM1)
  - 1 x 32-bit general-purpose timer (TIM2)
  - 5 x 16-bit general-purpose timers (TIM3/14/15/16/17)
  - 2 x basic timers (TIM6/TIM7)
  - 1 x low power timer (LPTIM)
  - 1 x independent watchdog timer (IWDG)
  - 1 x window watchdog timer (WWDG)
  - 1 x SysTick timer
- RTC
- Communication interfaces
  - 2 x serial peripheral interfaces (SPIs) with I^2S function
  - 4 x universal synchronous/asynchronous Transceivers (USARTs) , support automatic baud rate detection, two of USARTs support ISO7816, LIN and IrDA
  - 2 x I^2C interfaces supporting standard mode (100 kHz), Fast mode (400 kHz), 7-bit/10-bit addressing mode and SMBus
  - USB 2.0 full-speed interface
  - CAN 2.0 standard communication interface
- Hardware CRC-32 module
- Hardware 32-bit divider（DIV）
- Unique UID
- Serial wire debug (SWD)
- Operating temperature: - 40 ~ 105 ℃
- Packages: LQFP64,LQFP48,QFN48,QFN32(4*4)

Content

1. Introduction

The PY32F072-E microcontrollers incorporate the high-performance ARM® 32-bit Cortex®-M0+ core operating at up to 72 MHz frequency,embedded memories with up to 128 KB Flash and 16 KB SRAM, and contains various products in different package types. The chip integrates multi-channel I^2C, SPI, USART and other communication peripherals, one 12-bit ADC, two DACs, 13 timers, one USB 2.0, one CAN 2.0, three comparators, three operational amplifiers, and one LCD driver.

The PY32F072-E microcontrollers operate in the -40 to 105 °C temperature range, from a 1.7 to 5.5 V power supply,provides Sleep and Stop low-power operating modes, which can meet different low-power applications.

These features make the PY32F072-E microcontrollers suitable for a wide range of applications such as controllers, portable devices, PC peripherals, gaming and GPS platforms, industrial applications.

Table 1-1 PY32F072-E series product features and peripheral counts

Peripherals		PY32F072R1BT7-E	PY32F072C1BT7-E	PY32F072C1BU7-E	PY32F072K3BU7-E
Flash (KB)		128	128	128	128
SRAM (KB)		16	16	16	16
Timers	Advanced control	1 (16-bit)			
	General purpose	5 (16-bit)			
		1(32-bit)			
	Basic	2			
	Low power	1			
	SysTick	1			
	Watchdog	2			
Comm. interfaces	SPI[I^2S]	2[2]			
	I^2C	2			
	USART	4			
	CAN	1			
	USB	1			
DMA		7ch			
RTC		Yes			
GPIOs		58	42	42	28
12-bit ADC (external + internal)		1 (16 + 8)	1 (10 + 8)	1 (10 + 8)	1 (10 + 8)
12-bit DAC (Channels)		2 (2)			
Comparators		3			
OPA		3			2
LCD		1			
Max. CPU frequency		72 MHz			
Operating voltage		1.7 - 5.5 V			
Operating temperature		- 40 ~ 105 °C			
Packages		LQFP64	LQFP48	QFN48	QFN32(4*4)

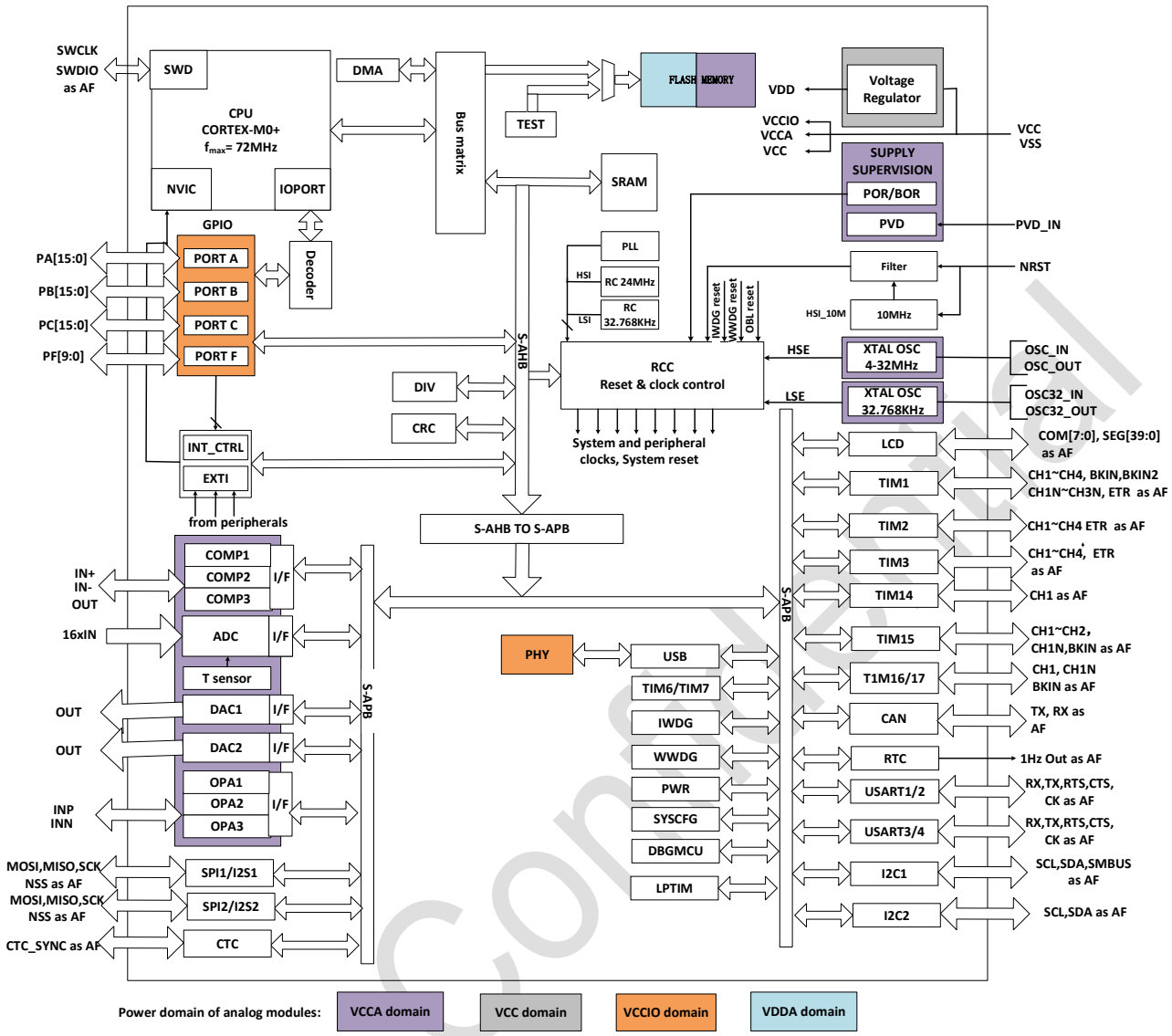


Figure 1-1 System block diagram

2. Functional Overview

2.1. Arm®-Cortex®-M0+ core

The Arm® Cortex® -M0+ is an entry-level Arm 32-bit Cortex processor designed for embedded applications. It provides developers with significant benefits, including:

- Simple structure, easy to learn and program
- Ultra-low power consumption, energy-saving operation
- Reduced code density and more

The Arm® Cortex-M0+ processor is a 32-bit core optimized for area and power consumption and is a 2-stage pipeline Von Neumann architecture. The processor offers high-end processing hardware, including single-cycle multipliers, through a streamlined but powerful instruction set and an extensively optimized design. Moreover, it delivers the superior performance expected from a 32-bit architecture computer, with a higher coding density than other 8 and 16-bit microcontrollers.

The Cortex-M0+ is tightly coupled with a Nested Vectored Interrupt Controller (NVIC).

2.2. Memories

16 KB of embedded SRAM accessed by Bytes (8 bits), Half-word (16 bits) or Word (32 bits).

The non-volatile memory is divided into two arrays:

- 128 KB of Main flash area for programs and data
- 14 KB of Information area:
  - FT info0 bytes
  - Option bytes
  - UID bytes
  - System memory

The protection of Main flash area includes the following mechanisms:

- Read protection (RDP) prevents outside access.
- Write protection (WRP) prevents unwanted write operation (caused by confusion of program memory pointer from PC). The minimum protection unit for write protection is 8 KB .
- Option byte write protection is a special design for unlock.

2.3. Boot modes

At startup, the BOOT0 pin and boot selector option bit nBOOT are used to select one of the three boot options in the following table:

Table 2-1 Boot configuration

Boot mode configuration		Mode
nBOOT1 bit	BOOT0 pin	
X	0	Boot from Main flash
1	1	Boot from System memory
0	1	Boot from SRAM

The Boot loader is located in the System memory and is used to reprogram the Flash memory by using USART or USB interface.

2.4. Clock system

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset.After the program is operating the system clock frequency and system clock source can be reconfigured. The frequency clocks that can be selected are:

- A 4/8/16/22.12/24 MHz configurable internal high precision HSI clock
- A 32.768 kHz configurable internal LSI clock
- A 4 to 32 MHz HSE clock, and used to enable the CSS function to detect HSE. If CSS fails, the hardware will automatically convert the system clock to HSI, and software configures the HSI frequency. Simultaneously, CPU NMI interrupt is generated.
- A 32.768 kHz LSE clock.
- PLL clock has HSI and HSE sources. If the HSE source is selected, when CSS is enabled and CSS fails, the PLL and HSE will be turned off, and the hardware selects the system clock source as HSI.

The AHB clock can be divided based on the system clock, and the APB clock can be divided based on the AHB clock. The maximum frequency of the AHB and the APB domains is 72 MHz.

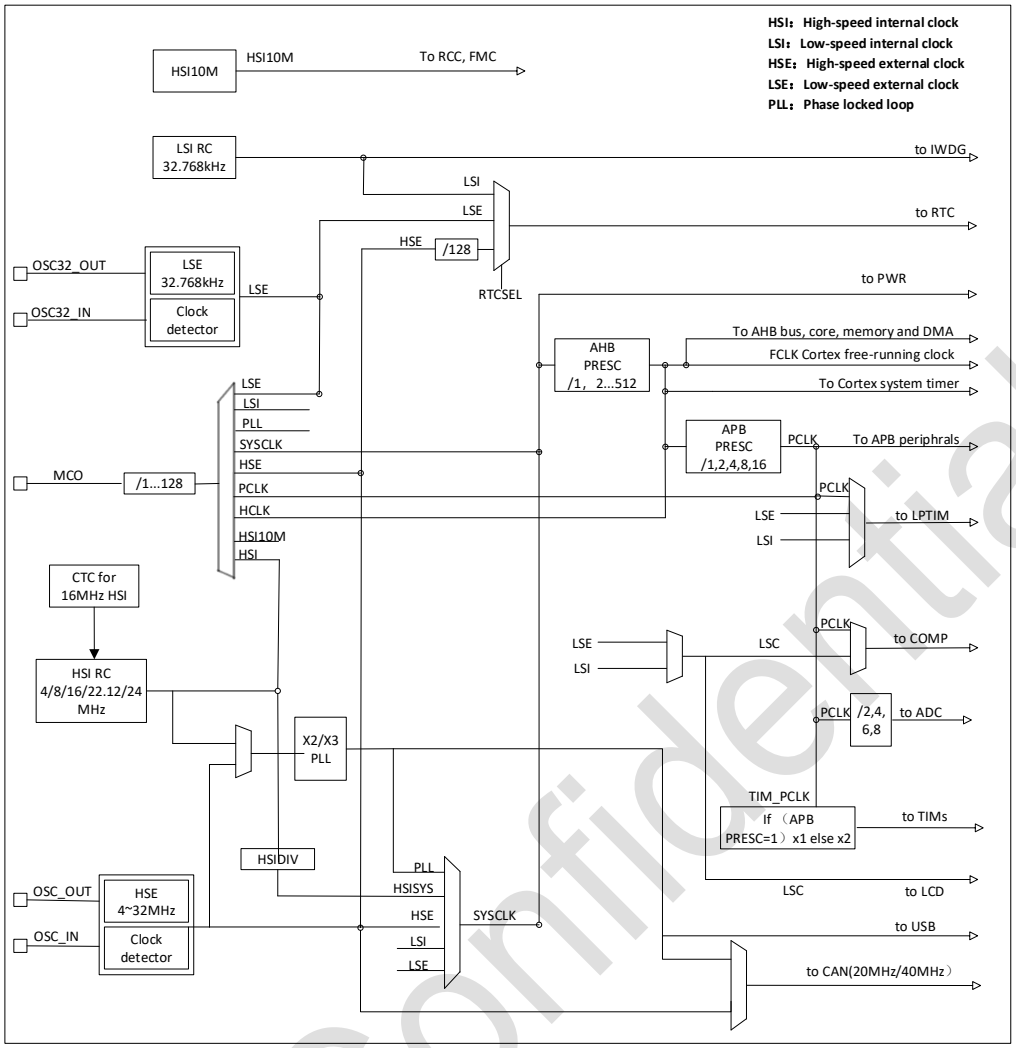


Figure 2-1 System clock structure diagram

2.5. Power management

2.5.1. Power block diagram

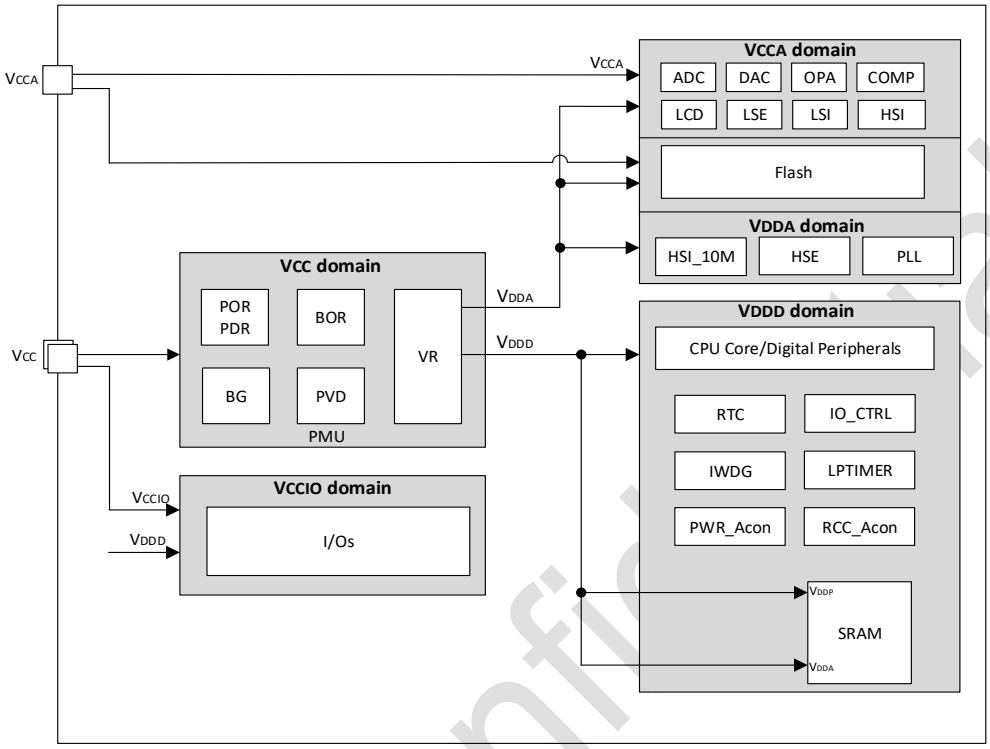


Figure 2-2 Power block diagram

Table 2-2 Power block diagram

No.	Power supply	Power value	Descriptions
1	V_{CC}	1.7 to 5.5 V	External power supply for I/Os and the internal regulator. It is provided externally through V_{CC} pins.
2	V_{CCA}	1.7 to 5.5 V	External analog power supply for ADC, DAC, COMP,OPA,LCD,RCs and PLL.It is provided externally through V_{CCA} pins.
3	V_{DDx} (V_{DDD}/V_{DDA})	1.2 V/1.0 V/0.9 V/0.8 V	VR supplies power to the main logic circuits and SRAM inside the chip. When the MR is powered, it outputs 1.2 V. According to the software configuration, when entering the Stop mode it powered by MR or LPR, and the LPR output is determined to be 1.2 V/1.0 V/0.9 V/0.8 V.

2.5.2. Power monitoring

2.5.2.1. Power on reset (POR/PDR)

The power-on reset (POR) and power-down reset (PDR) module is designed in the chip to provide power-on and power-off reset for the chip. The module keeps working in all modes.

2.5.2.2. Brown-out reset (BOR)

In addition to POR/ PDR, BOR (Brown-out reset) is also implemented. BOR can only be enabled and disabled through the option byte .

When the BOR is turned on, the BOR threshold can be selected by the option byte and both the rising and falling detection points can be individually configured.

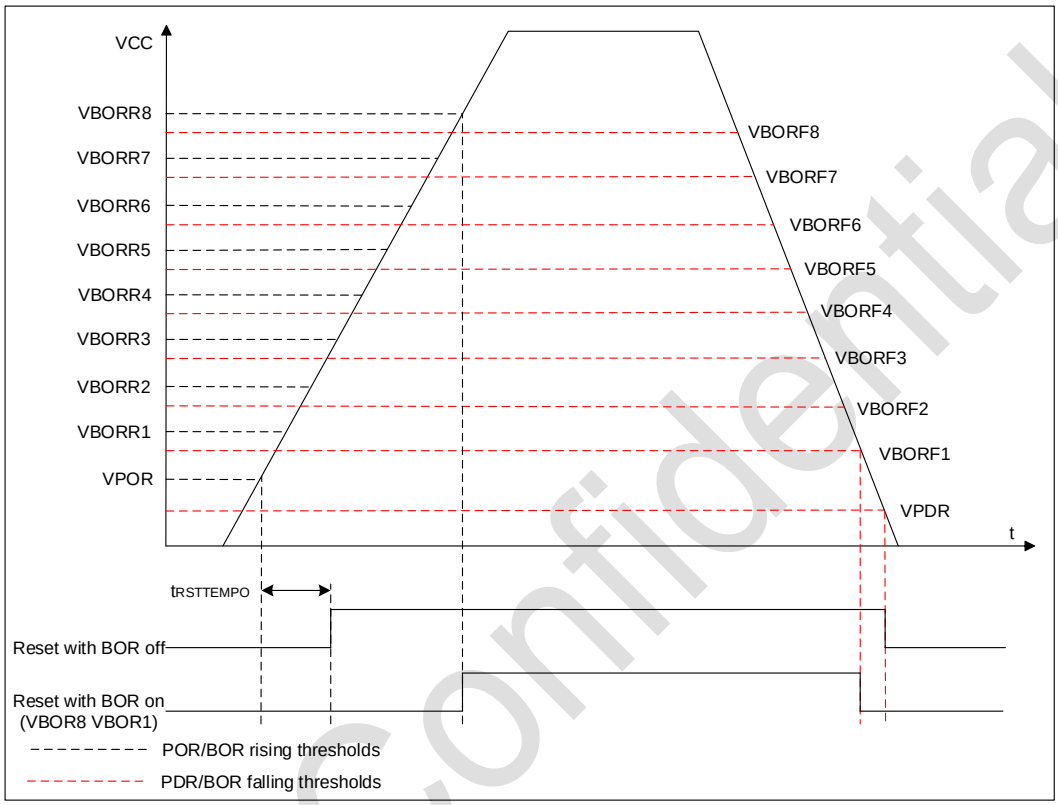


Figure 2-3 POR/PDR/BOR threshold

2.5.2.3. Programmable voltage detector (PVD)

Programmable voltage detector (PVD) module can be used to detect the V_{CC} power supply and the voltage of the PB7 pin, and the detection point is configured through the register. When V_{CC} is higher or lower than the detection point of PVD , the corresponding reset flag is generated.

This event is internally connected to line 16 of EXTI , depending on the rising/falling edge configuration of EXTI line 16, when V_{CC} rises above the detection point of PVD, or V_{CC} falls below the detection point of PVD, an interrupt is generated. In the service program, users can perform urgent shutdown tasks.

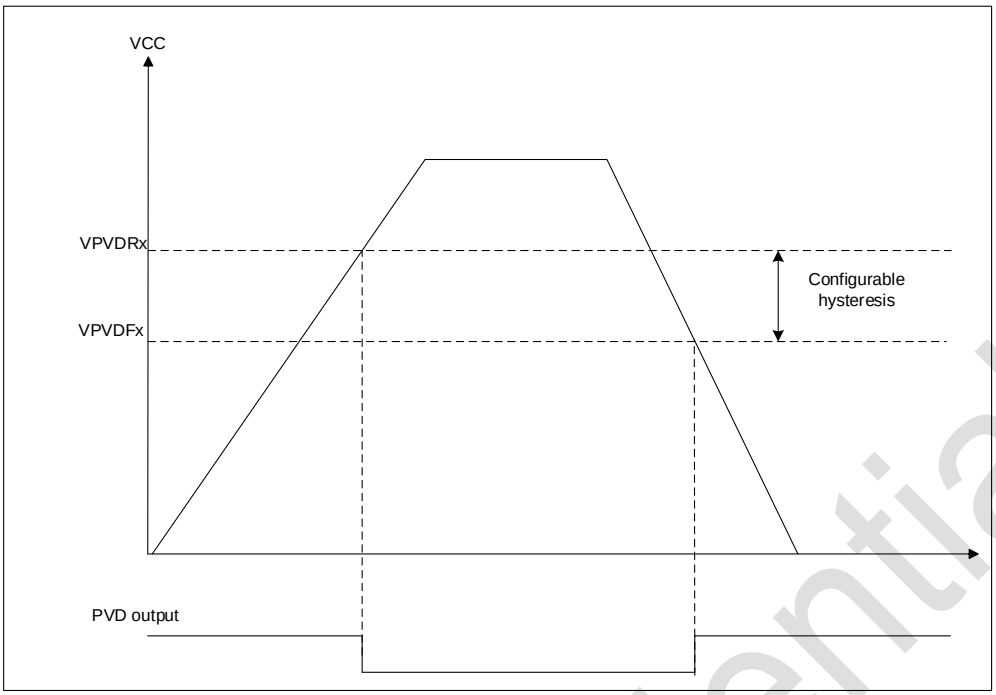


Figure 2-4 PVD threshold

2.5.3. Voltage regulator

The regulator has two operating modes:

- Main regulator (MR) is used in normal operating mode(Run).
- Low power regulator (LPR) can be used in Stop mode where the power demand is reduced.

2.5.4. Low-power mode

In addition to the normal operating mode, the chip has 2 low-power modes:

- Sleep mode: Peripherals can be configured to keep working when the CPU clock is off (NVIC, SysTick, etc.). It is recommended only to enable the modules that must work, and close the module after the module works.
- Stop mode: In this mode, the contents of SRAM and registers are maintained, HSI and HSE are turned off, and most modules of clocks in the V_{DD} domain are stopped. GPIO, PVD, COMP output, RTC and LPTIM can wake up Stop mode.

2.6. Reset

Two resets are designed in the chip: power reset and system reset.

2.6.1. Power reset

A power reset occurs in the following situations:

- Power-on/power-down reset (POR/PDR)
- Brown-out Reset (BOR)

2.6.2. System reset

A system reset occurs when the following events occur:

- Reset of NRST pin
- Windowed watchdog reset (WWDG)
- Independent watchdog reset (IWDG)
- SYSRESETREQ software reset
- Option byte load reset (OBL)

2.7. General-purpose inputs and outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function.The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.8. Direct memory access controller (DMA)

Direct memory access (DMA) is used to provide a high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps the CPU resources free for other operations.

The DMA controller have 7 channels in total, each one dedicated to manage memory access requests from one or more peripherals. Each controller has an arbiter for handling the priority between DMA requests.

The DMA supports:

- Single AHB Master
- Support peripherals to memory, the memory to the peripherals, memory to memory and peripherals to peripheral data transmission
- On-chip memory devices, such as Flash, an SRAM, AHB and APB peripherals, as the source and target
- All DMA channel can be independent configuration:
  - Each channel is associated either with a DMA request signal from a peripheral or with a software trigger in a memory-to-memory transfer. This configuration is done by software.
  - The priority between requests is programmable by software (4 levels per channel: very high, high, medium and low) and, in equal cases, by hardware (such as a request for channel 1 taking precedence over a request for channel 2).
  - The transfer sizes of the source and destination are independent (byte, half word and word), simulating packing and unpacking. The source and destination addresses must be aligned by data size.
  - Programmable number of data to be transferred:0 ~ 65535
- Each channel generates an interrupt request. Each interrupt request is caused by one of three DMA events: transfer completion, half-transfer, or transfer error.

2.9. Interrupts and events

The PY32F072-E handles exceptions through the Cortex-M0+ processor's embedded a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI).

2.9.1. Nested vectored interrupt controller (NVIC)

NVIC is a tightly coupled IP inside the Cortex-M0+ processor. The NVIC can handle NMI (Non-Maskable Interrupts) and maskable external interrupts from outside the processor and Cortex-M0+ internal exceptions. NVIC provides flexible priority management.

The tight coupling of the processor core to the NVIC greatly reduces the delay between an interrupt event and the initiation of the corresponding interrupt service routine (ISR). The ISR vectors are listed in a vector table, stored at a base address of the NVIC. The vector table base address determines the vector address of the ISR to execute, and the ISR is used as the offset composed of serial numbers.

If a higher-priority interrupt event occurs and a lower-priority interrupt event is just waiting to be serviced, the later-arriving higher-priority interrupt event will be serviced first. Another optimization is called tail-chaining. When returning from a higher-priority ISR and then starting a pending lower-priority ISR, unnecessary pushes and pops of processor contexts will be skipped. This reduces latency and improves power efficiency.

NVIC features:

- Low latency interrupt handling
- Level 4 interrupt priority
- Supports one NMI interrupt
- Support 32 maskable external interrupts
- High-priority interrupts can interrupt low-priority interrupt responses
- Support tail-chaining optimization
- Hardware interrupt vector retrieval

2.9.2. Extended interrupt/event controller (EXTI)

EXTI adds flexibility to handle physical wire events and generates wake-up events when the processor wakes up from Stop mode.

The EXTI controller has multiple channels, including a maximum of 16 GPIOs, 1 PVD output, 3 COMP outputs, RTC and LPTIM wake-up signals. GPIO, PVD and COMP can be configured to be triggered by a rising edge, falling edge or double edge. Any GPIO signal can be configured as EXTI0 to 15 channel through the select signal.

- Each EXTI line can be independently masked through registers.
- The EXTI controller can capture pulses shorter than the internal clock period.
- Registers in the EXTI controller latch each event. Even in Stop mode, after the processor wakes up from Stop mode, it can identify the wake-up source or identify the GPIO and event that caused the interrupt.

2.10. Analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter has up to 16 external and 8 internal channels.

The ADC internal voltage reference: V_{REFBUF}(1.5 V,2.048 V,2.5 V) or the power supply voltage V_{CCA}.

The internal channels are： T_{S_VIN},V_{REFINT},V_{CCA}/3,OPA 1~3 and DAC 1~2.

- A/D conversion of the various channels can be performed in single,continuous,scan or
- discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.
- The analog watchdog feature allows the application to detect if the input voltage goes
- outside the user-defined higher or lower thresholds.
- An efficient low-power mode is implemented to allow very low consumption at low frequency.
- Analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers

2.11. Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs.The DAC can be configured in 8-bit or 12-bit mode, or can be used in conjunction with a DMA controller. When the DAC is operating in 12-bit mode, the data can be left justified or right justified. The DAC module has two output channels, each with a separate converter. In dual-DAC mode, the two channels can be converted independently, or they can be converted simultaneously and update the output of the two channels synchronously. The main features are as follows:

- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- Support DMA underflow error detection
- External triggers for conversion

2.12. Comparators (COMP)

The COMP1/2/3 module can be used as a separate module or in combination with timer. Comparators can be used as：

- Triggered by analog signal to wake-up function from low-power mode
- Analog signal conditioning
- Cycle by cycle current control loop when comparators are connected with PWM output from timer.

COMP features are summarized as follows:

- Voltage comparison function is supported. Each comparator has configurable positive or negative input for flexible voltage selection:

  - Multiple I/O pins
  - 64 steps voltage of V_{CCA}/V_{REFBUF}/V_{REF1P2}
  - Temperature sensor output
  - DAC output
  - OPA output
- Programmable speed and power consumption
- Rail to Rail
- Hysteresis function
- The output can be triggered by a connection to the I/O or timer input
- Each COMP has interrupt generation capability and is used to wake up the chip from low power mode (Sleep/Stop) (via EXTI)
- Provides software to configure the digital filtering time to enhance the anti-interference capability of the chip
- Supports the Window Comp function

2.13. Operational amplifier (OPA)

The OPA1/2/3 module can be flexibly configured and is suitable for simple amplifiers. The three internal OPA can be cascaded using external resistors.

OPA features are summarized as follows:

- Three independently configured operational amps
- OPA input range is 0 to V_{CCA}, output range is 0.1 V to V_{CCA} - 0.2 V (demand) to simulate a module, a programmable gain
- Can be configured for the following models
  - General operational mode (general purpose OPA)

2.14. Liquid crystal display (LCD) controller

The LCD controller is a digital controller/driver for monochrome passive liquid crystal displays (LCD), with up to 8 common terminals (COM) and 40 segment terminals (SEG) to drive 160 (4 * 40) or 288 (8 * 36) LCD pixels. The exact number of terminals depends on the device pins described in the data manual. LCD functions are summarized as follows:

- Highly flexible frame rate control
- Support static, 1/2, 1/3, 1/4, 1/6, and 1/8 of a duty ratio
- Support static, 1/2, 1/3 bias voltage
- Up to 16 registers LCD data RAM
- By software configuration of LCD contrast
- 2 kinds of waveform generation
  - Internal resistance divider, external resistance divider
  - By way of internal resistance of the software configuration partial pressure power consumption, so as to match the capacitance charge needed for the LCD panel
- Support low power consumption modes: LCD controller can be on the Run, Sleep and Stop

mode for display

- Configurable frame interrupt
- Support LCD flashing function and configuration of multiple flicker frequency configuration
- Unused LCD segments and public pin can be configured to digital or analog functions

2.15. Hardware divider (DIV)

Hardware divider is a 32-bit signed/unsigned integer hardware divider.

DIV features:

- Support 32-bit division
- The data in the register cannot be changed while the current division is not finished
- Configurable signed/unsigned integer division calculation
- 32-bit divisor, 32-bit divisor
- Outputs 32-bit quotient and 32-bit remainder
- Divide-by-zero warning flag bit, end-of-division flag bit
- 8 clock cycles to complete a division operation
- Write the divisor register to trigger the start of the division circuit
- After writing the divisor, when reading the quotient and remainder registers, you need to wait for the completion flag DIV_END
- When the divisor is 0, the result of quotient and remainder is 0

2.16. Timers

Table 2-3 compares the features of the different timers.

Table 2-3 Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA	Capture /compare channels	Complemen-tary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	Integer from 1 to 65536	Yes	4	3
General purpose	TIM2	32-bit	Up, down, up/down	Integer from 1 to 65536	Yes	4	-
General purpose	TIM3	16-bit	Up, down, up/down	Integer from 1 to 65536	Yes	4	-
	TIM14	16-bit	Up	Integer from 1 to 65536	-	1	-
	TIM15	16-bit	Up	Integer from 1 to 65536	Yes	2	1
	TIM16 TIM17	16-bit	Up	Integer from 1 to 65536	Yes	1	1
Basic	TIM6 TIM7	16-bit	Up	Integer from 1 to 65536	Yes	-	-

2.16.1. Advanced-control timer (TIM1)

The advanced-control timer (TIM1) is consist of a 16-bit auto-reload counter driven by a programmable prescaler. It can be used in various scenarios, including pulse length measurement of input signals (input capture) or generating output waveforms (output compare, output PWM, complementary PWM with dead-time insertion).

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned mode)
- Single pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers by the Timer Link feature for synchronization or event chaining.

TIM1 supports the DMA function.

2.16.2. General-purpose timers

2.16.2.1. TIM2/TIM3

The general-purpose timers TIM2/TIM3 are consist of 32/16-bit auto-reload counters and a 32/16-bit prescaler. There are four independent channels each for input capture/output compare, PWM or one-pulse mode output.

- They can work with the TIM1 by the Timer Link.
- TIM2/TIM3 supports DMA function.
- This timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.
- The counter can be frozen in debug mode.

2.16.2.2. TIM14

- The general-purpose timer TIM14 is consist of a 16-bit auto-reload counter driven by a programmable prescaler.
- TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.
- The counter can be frozen in debug mode.

2.16.2.3. TIM15/TIM16/TIM17

- The general-purpose timer (TIM15, TIM16 and TIM17) is consist of a 16-bit auto-reload counter driven by a programmable prescaler.
- TIM16/TIM17 features one single channel for input capture/output compare, PWM or one-pulse mode output.
- TIM15 features two single channel for input capture/output compare, PWM or one-pulse mode output.
- TIM15/TIM16/TIM17 have complementary outputs with dead time.
- TIM15/TIM16/TIM17 supports DMA function.

- The counter can be frozen in debug mode.

2.16.3. Basic timers (TIM6/TIM7)

- The basic timer TIM6/TIM7 is consist of a 16-bit auto-reload upcounter driven by their programmable prescaler respectively.
- Synchronization circuit to trigger DAC.
- Generate interrupt/DMA request on update event (counter overflow).

2.16.4. Low power timer (LPTIM)

- LPTIM is a 16 -bit upcounter with a 3-bit prescaler and support a continuous or single count.
- LPTIM can be configured as a Stop mode wake-up source.
- The counter can be frozen in debug mode.

2.16.5. Independent watchdog (IWDG)

Independent watchdog (IWDG) is integrated in the chip, and this module has the characteristics of high-security level, accurate timing and flexible use. IWDG finds and resolves functional confusion due to software failure and triggers a system reset when the counter reaches the specified timeout value.

- The IWDG is clocked by LSI, so even if the main clock fails, it can keep working.
- IWDG is the best suited for applications that require the watchdog as a standalone process outside of the main application and do not have high timing accuracy constraints.
- Controlling of option byte can enable IWDG hardware mode.
- IWDG is the wake-up source of Stop mode, which wakes up Stop mode by reset.
- The counter can be frozen in debug mode.

2.16.6. System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability, and the counter can be frozen in debug mode.

2.16.7. SysTick timer

SysTick timer is dedicated to real-time operating systems, but could also be used as a standard down counter.

SysTick features:

- A 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0

2.17. Real-time clock (RTC)

The RTC is an independent counter. It has a set of continuous counting counters, which can provide a clock calendar function under the corresponding software configuration. Modifying the value of the counter can reset the current time and date of the system.

- RTC is a 32-bit programmable counter with a prescaler factor of up to 2^{20} bits.
- The RTC counter clock source can be LSE,LSI and HSE/128.
- RTC can generate alarm interrupt, second interrupt and overflow interrupt (maskable).
- RTC supports clock calibration.
- RTC can be frozen in debug mode.

2.18. Cyclic redundancy check calculation unit(CRC)

CRC computing unit is based on a fixed generation polynomial to obtain 32-bit CRC computing results. In other applications, CRC technology is mainly used to verify the correctness and integrity of data transmission or data storage.

2.19. Clock trimming controller(CTC)

The clock calibration controller (CTC) uses hardware to automatically calibrate the RC crystal oscillator (HSI) when the internal configuration is 16 MHz, and uses the PLL (48 MHz) after 3 times the frequency as the clock source of the USBD module. The CTC module calibrates the HSI clock frequency based on an external high-precision reference signal source, and adjusts the calibration value automatically or manually to obtain an accurate PLL48 MHz clock.

The CTC module performs the following functions:

- Three external reference sources: GPIO,LSE clock and USBD_SOF.
- Provide software reference synchronization pulse.
- Hardware calibration automatically, no software operation.
- 16 bits calibration counter with reference source capture and overload capabilities.
- 8 bits clock calibration base value for frequency evaluation and automatic calibration.
- Flag bits and interrupts that indicate the state of clock calibration: calibration success state (CKOKIF), warning state (CKWARNIF), and error state (ERRIF).

2.20. System configuration controller (SYSCFG)

The SYSCFG module provides the following functions:

- Enable and disable I^2C type IO filter
- Mapping the initial program area according to different boot modes
- DMA peripheral channel selection control
- TIMx cascade control
- Enable and disable PVD Lock
- Enable and disable Cortex-M0+ LOCKUP
- Enable and disable Noise filter for all GPIOs

2.21. Debug support（DBG）

The MCU DBG module assists the debugger with the following functions:

- Support Sleep mode, Stop mode

- When the CPU enters the HALT mode, the control timer or watchdog stops counting or continues counting
- Block I²C1 and I²C2 SMBUS timeouts when the CPU is in HALT mode
- Block CAN receive register updates when the CPU is in HALT mode
- Assigns tracking pins

The MCUDBG register also provides chip ID encoding. This ID encoding can be accessed by a JTAG or SW debug interface, or by a user program.

2.22. Inter-integrated circuit interface (I²C)

The I2C (inter-integrated circuit) bus interface handles communications between the microcontroller and the serial I2C bus. It provides multimaster capability, and controls all I2C bus-specific sequencing, protocol, arbitration and timing. It supports Standard-mode (Sm) and Fast-mode (Fm) .

I²C features:

- Two I²C Interfaces
- Multimaster capability : can be Master or Slave
- Support different communication speeds
  - Standard Mode (Sm): up to 100 kHz
  - Fast Mode (Fm): up to 400 kHz
- As Master
  - Generate Clock
  - Generation of Start and Stop
- As Slave
  - Programmable I²C address detection
  - Dual-address capability that responds to two secondary addresses
  - Discovery of the Stop bit
- 7-bit/10-bit addressing mode
- General call
- Status flag
  - Transmit/receive mode flags
  - Byte transfer complete flag
  - I²C busy flag bit
- Error flag
  - Master arbitration loss
  - ACK failure after address/data transfer
  - Start/stop error
  - Overrun/Underrun (clock stretching function disable)
- Optional clock stretching
- Single-byte buffer with DMA capability
- Software reset
- Analog noise filter function

- Hardware PEC (packet error checking) generation and verification with ACK control
- Support SMBus

2.23. Universal synchronous/asynchronous receiver transmitter (USART)

PY32F072-E contains 4 USARTs,two of USARTs(USART1 and USART2) support ISO7816, LIN , and IrDA.

The USARTs provide a flexible method for full-duplex data exchange with external devices using the industry-standard NRZ asynchronous serial data format. The USART utilizes a fractional baud rate generator to provide a wide range of baud rate options.

It supports simultaneous one-way communication and half-duplex single-wire communication, and it also allows multi-processor communication.

Automatic baud rate detection is supported.

High-speed data communication can be achieved by using the DMA method of the multi-buffer configuration.

USARTs features:

- Full-duplex asynchronous communication
- NRZ standard format
- Configurable 16 times or 8 times oversampling for increased flexibility in speed and clock tolerance
- Programmable baud rate shared by transmit and receive, up to 4.5 Mbit/s
- Automatic baud rate detection
- Programmable data length of 8 or 9 bits
- Configurable stop bits (0.5,1,1 or 2 bits)
- Synchronous mode and clock output function for synchronous communication
- Single-wire half-duplex communication
- Independent transmit and receive enable bits
- Hardware flow control
- Receive/transmit bytes by DMA buffer
- Detection flag
  - Receive full buffer
  - Send empty buffer
  - End of transmission
- Parity control
  - Send check digit
  - Check the received data
- Flagged interrupt sources
  - CTS change
  - Send empty register

  - Send completed
  - Receive full data register
  - Bus idle detected
  - Overflow error
  - Frame error
  - Noise operation
  - Error detection
- Multiprocessor communication
  - If the address does not match, enter silent mode
- Wake-up from silent mode: by idle detection and address flag detection

2.24. Serial peripheral interface (SPI)

PY32F072-E contains two SPIs. SPIs allow the chip to communicate with external devices in half-duplex, full-duplex, and simplex synchronous serial communication. This interface can be configured in Master mode and provides the serial clock (SCK) for external slave devices. The interface can also work in a multi-master configuration.

The SPI features are as follows:

- Master or Slave mode
- 3-wire full-duplex simultaneous transmission
- 2-wire half-duplex synchronous transmission (with bidirectional data line)
- 2-wire simplex synchronous transmission (no bidirectional data line)
- 8-bit or 16-bit transmission frame selection
- Support multi-master mode
- 8 Master mode baud rate prescale factors (Max $f_{PCLK}/2$)
- Slave mode frequency (Max $f_{PCLK}/4$)
- Both Master and Slave modes can be managed by software or hardware NSS: dynamic change of Master/Slave operating mode
- Programmable clock polarity and phase
- Programmable data order, MSB first or LSB first
- Dedicated transmit and receive flags that can trigger interrupts
- SPI bus busy status flag
- Motorola mode
- Interrupt-causing Master mode faults or overloads
- Two 32-bit Rx and Tx FIFOs with DMA capability

2.25. USB 2.0 full-speed module

PY32F072-E contains 1 USB 2.0 full speed module. USB peripheral implements the interface between USB2.0 full speed bus and APB1 bus. It supports USB suspend/restore operation and can stop the device clock to achieve low power consumption. The main features are as follows:

- Comply with the technical specifications of USB 2.0 full speed devices

- It can be configured with 1 to 6 USB endpoints
- CRC (cyclic redundancy check) generation/check, reverse non-return to zero inverted (NRZI) encoding/decoding and bit filling
- Support control transmission/synchronous transmission/batch transmission/interrupt transmission
- Support a dual buffer mechanism for batch/synchronous endpoints
- USB suspend and restore operations are supported
- Frame lock clock pulse generation
- Dedicated 1024 Bytes packet cache storage

2.26. CAN 2.0

PY32F072-E contains one CAN communication interface module. The Controller Area Network (CAN) bus is a bus standard that can realize the communication between microprocessors or devices without a host.

The CAN bus controller can handle data sending and receiving on the bus. In this product, the CAN controller has 12 groups of filters. Filters are used to select messages for the application to receive. The application program in the CAN controller can transmit 1 Primary Transmit Buffer (PTB) and 3 Secondary Transmit buffers (STB) which help to send the sending data to the bus, and the sending scheduler determines the sending order of the mailboxes. The bus data is obtained through three Receive Buffers (RB). Three STBs and three RBs can be interpreted as two level-3 FIFO, where the FIFO is completely hardware controlled. The CAN bus controller also supports Time-trigger communication.

- Fully support ISO11898-1 CAN2.0A/ CAN2.0B protocol
- CAN 2.0 supports a maximum communication baud rate of 1Mbit/s
- The baud rate ranges from 1 to 1/32. The baud rate is flexibly configured
- Three receive buffers
  - FIFO mode
  - Error or non-received data does not overwrite stored messages
- One high - priority primary send buffer PTB
- Three sub-send buffers STB
  - FIFO mode
  - Priority arbitration mode
- 12 separate sets of filters
  - It supports 11-bit standard ID and 29-bit extended ID
  - Programmable ID CODE bit and MASK bit
- Support silent mode
- Support loopback mode
- Support capturing transmission error types and locating quorum failure locations
- Programmable error warning value
- Support ISO11898-4 time trigger CAN and receive time stamp

2.27. Serial wire debug (SWD)

An ARM SWD interface allows serial debugging tools to be connected to the PY32F072-E.

3. Pinouts and pin descriptions

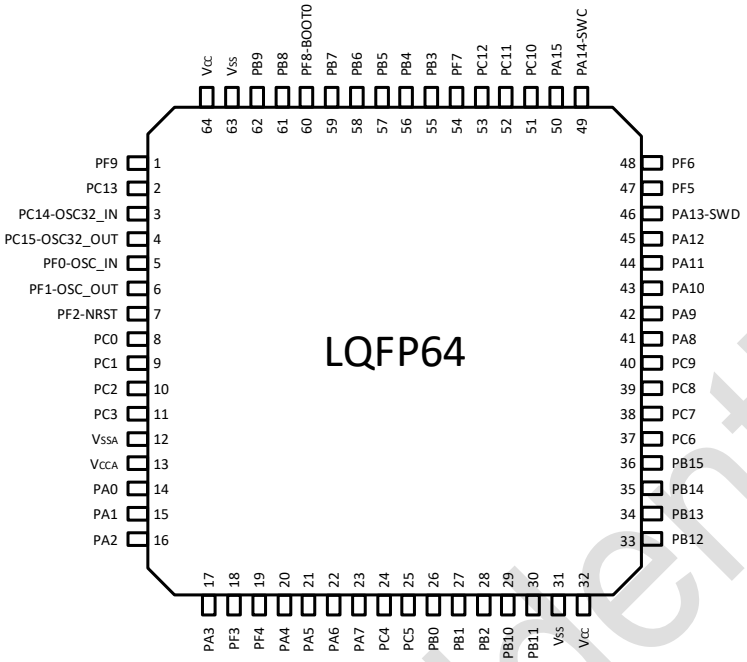


Figure 3-1 LQFP64 PY32F072R1xT7-E Pinout1 (Top view)

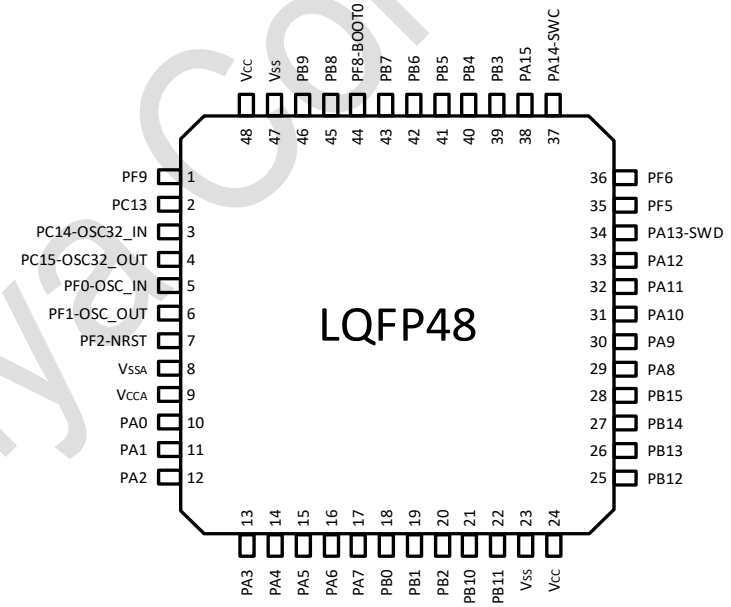


Figure3-2 LQFP48 PY32F072C1xT7-E Pinout1 (Top view)

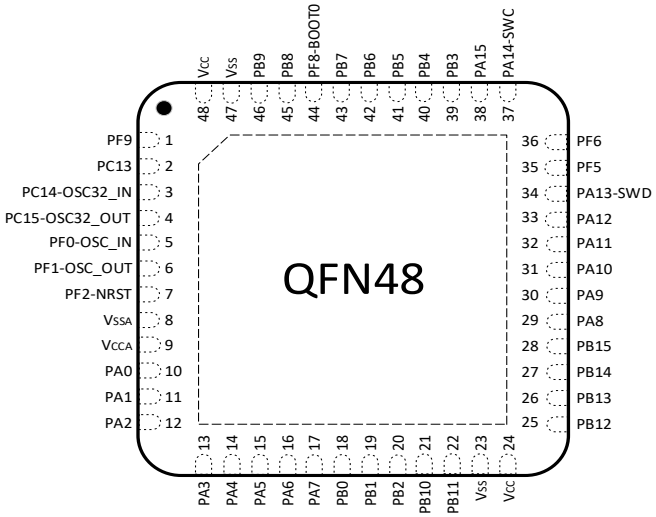


Figure3-3 QFN48 PY32F072C1xU7-E Pinout1 (Top view)

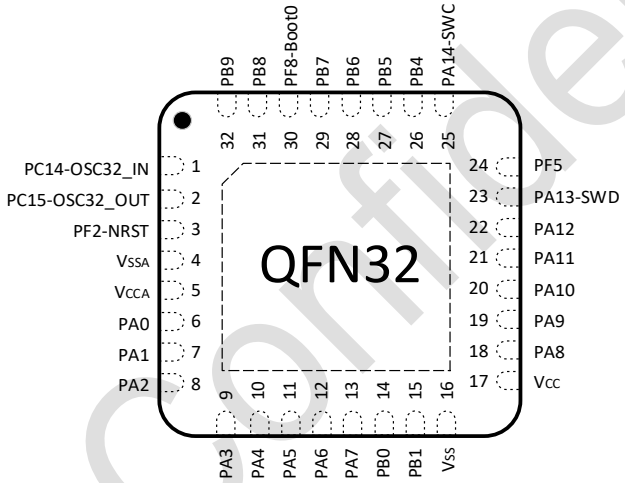


Figure3-4 QFN32(4*4) PY32F072K3xU7-E Pinout3 (Top view)

Table 3-1 Legend/abbreviations used in the pinout table

Name		Symbol	Definition
Pin type		S	Supply pin
		G	Ground pin
		I	Input-only pin
		I/O	Input / output pin
I/O structure		COM	Standard 5V I/O,with Analog switch function supplied by V_{CCA}
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		COM_U	I/O, with USB PHY function
Notes		-	Unless otherwise specified, all ports are used as floating inputs between and after reset
Pin functions	Alternate functions	-	Function selected through GPIOx_AFR register
	Additional functions	-	Functions directly selected/enabled through peripheral registers

Table 3-2 Pin definitions

Packages				Reset	Port type	Port structure	Notes	Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K3					Alternate functions	Additional functions
1	1	1	-	PF9	I/O	COM		-	-
2	2	2	-	PC13	I/O	COM		SPI1_SCK/I²S1_CK	-
								TIM1_BKIN	
3	3	3	1	PC14	I/O	COM		TIM1_BKIN2	OSC32_IN
4	4	4	2	PC15	I/O	COM		TIM15_BKIN	OSC32_OUT
5	5	5	-	PF0-OSC_IN	I/O	COM		CTC_SYNC	OSC_IN
								USART2_TX	
								TIM1_BKIN	
								TIM14_CH1	
6	6	6	-	PF1-OSC_OUT	I/O	COM		USART2_RX	OSC_OUT
								TIM1_CH1N	
								TIM15_CH1N	
7	7	7	3	PF2-NRST	I/O	RST	(1)	TIM1_CH2	-
								EVENTOUT	
								MCO	
8	-	-	-	PC0	I/O	COM		EVENTOUT	ADC_IN10, COMP1_INN15, COMP2_INN0, SEG27
								SPI1_MISO/I²S1_MCK	
								USART2_CTS	
								USART3_RTS	
9	-	-	-	PC1	I/O	COM		EVENTOUT	ADC_IN11,

Packages				Reset	Port type	Port structure	Notes	Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K3					Alternate functions	Additional functions
								SPI1_MOSI/I²S1_SD	COMP1_INP1, COMP2_INN1, SEG26
								USART2_RTS	
								USART3_CTS	
								TIM15_CH1	
10	-	-	-	PC2	I/O	COM		EVENTOUT	ADC_IN12, COMP1_INP2, COMP2_INN2, SEG25
								SPI2_MISO/I²S2_MCK	
								USART3_TX	
								USART3_RX	
								TIM15_CH2	
11	-	-	-	PC3	I/O	COM		EVENTOUT	ADC_IN13, COMP1_INP3, COMP2_INN3, SEG24
								SPI2_MOSI/I²S2_SD	
								USART3_RX	
								USART3_TX	
12	8	8	4	V_{SSA}	G			Ground	
13	9	9	5	V_{CCA}	S			Analog power supply	
14	10	10	6	PA0	I/O	COM		USART2_CTS	ADC_IN0, COMP1_INP4, COMP1_INN0, COMP2_INP0, COMP2_INN4, SEG23
								TIM2_CH1_ETR	
								USART4_TX	
								COMP1_OUT	
								SPI2_SCK/I²S2_CK	
15	11	11	7	PA1	I/O	COM		EVENTOUT	ADC_IN1,

Packages				Reset	Port type	Port structure	Notes	Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K3					Alternate functions	Additional functions
								USART2_RTS	COMP1_INP5, COMP1_INN1, COMP2_INP1, COMP2_INN5, SEG22
								TIM2_CH2	
								USART4_RX	
								TIM15_CH1N	
								I^2C1_SMBA	
								SPI1_SCK/I^2S1_CK	
								SPI2_MOSI/I^2S2_SD	
16	12	12	8	PA2	I/O	COM		TIM15_CH1	ADC_IN2, COMP1_INP6, COMP1_INN2, COMP2_INP2, SEG21
								USART2_TX	
								TIM2_CH3	
								COMP2_OUT	
								SPI1_MOSI/I^2S1_SD	
								SPI2_MISO/I^2S2_MCK	
17	13	13	9	PA3	I/O	COM		EVENTOUT	ADC_IN3, COMP1_INP7, COMP1_INN3, COMP2_INP3, SEG20
								TIM15_CH2	
								USART2_RX	
								TIM2_CH4	
								SPI2_MISO/I^2S2_MCK	
								SPI2_NSS/I^2S2_WS	
18	-	-	-	PF3	I/O	COM		EVENTOUT	-
								I^2C1_SCL	

Packages				Reset	Port type	Port structure	Notes	Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K3					Alternate functions	Additional functions
								I^2C2_SCL	
19	-	-	-	PF4	I/O	COM		I^2C1_SDA	-
								I^2C2_SDA	
20	14	14	10	PA4	I/O	COM		EVENTOUT	ADC_IN4, DAC1_OUT, COMP1_INP8, COMP1_INN4, COMP2_INP4, SEG19
								SPI1_NSS/I^2S1_WS	
								USART2_CK	
								TIM14_CH1	
								SPI2_MOSI/I^2S2_SD	
								USART2_TX	
								PVD_OUT	
21	15	15	11	PA5	I/O	COM		EVENTOUT	ADC_IN5, DAC2_OUT, COMP1_INP9, COMP1_INN5, COMP2_INP5, COMP3_INP0, COMP3_INN0, SEG18, OPA2_OUT
								SPI1_SCK/I^2S1_CK	
								TIM2_CH1_ETR	
								USART3_TX	
22	16	16	12	PA6	I/O	COM		EVENTOUT	ADC_IN6, COMP1_INP10, COMP1_INN6, OPA2_INN,
								SPI1_MISO/I^2S1_MCK	
								TIM3_CH1	
								TIM1_BKIN	

Packages				Reset	Port type	Port structure	Notes	Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K3					Alternate functions	Additional functions
								USART3_CTS	SEG17
								TIM16_CH1	
								COMP1_OUT	
23	17	17	13	PA7	I/O	COM		EVENTOUT	ADC_IN7, COMP1_INP11, COMP1_INN7, OPA2_INP, SEG16
								SPI1_MOSI/I²S1_SD	
								TIM3_CH2	
								TIM1_CH1N	
								TIM14_CH1	
								TIM17_CH1	
								COMP2_OUT	
24	-	-	-	PC4	I/O	COM		EVENTOUT	ADC_IN14, COMP1_INN8, SEG15
								USART3_TX	
								COMP3_OUT	
								SPI1_NSS/I²S1_WS	
								USART1_TX	
								TIM2_CH1_ETR	
								IR_OUT	
25	-	-	-	PC5	I/O	COM		USART3_RX	ADC_IN15, COMP1_INN9, SEG14
								SPI1_MOSI/I²S1_SD	
								USART1_RX	
								TIM2_CH2	

Packages				Reset	Port type	Port structure	Notes	Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K3					Alternate functions	Additional functions
26	18	18	14	PB0	I/O	COM		EVENTOUT TIM3_CH3 TIM1_CH2N USART3_CK COMP1_OUT SPI1_NSS/I²S1_WS USART3_RX	ADC_IN8, COMP2_INN6, SEG13
27	19	19	15	PB1	I/O	COM		EVENTOUT TIM14_CH1 TIM3_CH4 TIM1_CH3N USART3_RTS COMP3_OUT	ADC_IN9, COMP2_INP6, COMP2_INN7, COMP3_INP1, COMP3_INN1, SEG12
28	20	20	-	PB2	I/O	COM		EVENTOUT SPI2_MISO/I²S2_MCK USART3_TX	COMP2_INP7, COMP2_INN8, SEG11
29	21	21	-	PB10	I/O	COM		I²C2_SCL TIM2_CH3 USART3_TX SPI2_SCK/I²S2_CK COMP1_OUT	COMP2_INP8, SEG10

Packages				Reset	Port type	Port structure	Notes	Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K3					Alternate functions	Additional functions
								USART2_RTS	
								I²C1_SCL	
30	22	22	-	PB11	I/O	COM		EVENTOUT	COMP3_INP2, COMP3_INN2, SEG9
								I²C2_SDA	
								TIM2_CH4	
								USART3_RX	
								COMP2_OUT	
								SPI2_MOSI/I²S2_SD	
								USART2_CTS	
								I²C1_SDA	
31	23	23	16	V_{SS}	G			Ground	
32	24	24	17	V_{CC}	S			Digital power supply	
33	25	25	-	PB12	I/O	COM		EVENTOUT	COMP2_INN15, OPA3_INN, SEG8
								SPI2_NSS/I²S2_WS	
								TIM1_BKIN	
								USART3_CK	
								TIM15_BKIN	
34	26	26	-	PB13	I/O	COM		EVENTOUT	COMP2_INP10, OPA3_INP, SEG7
								SPI2_SCK/I²S2_CK	
								TIM1_CH1N	
								USART3_CTS	

Packages				Reset	Port type	Port structure	Notes	Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K3					Alternate functions	Additional functions
								I^2C2_SCL	
								MCO	
								TIM15_CH1N	
								I^2C1_SCL	
35	27	27	-	PB14	I/O	COM		EVENTOUT	COMP2_INP11, COMP3_INP3, COMP3_INN3, OPA3_OUT, SEG6
								SPI2_MISO/I^2S2_MCK	
								TIM15_CH1	
								TIM1_CH2N	
								USART3_RTS	
								I^2C2_SDA	
								I^2C1_SDA	
36	28	28	-	PB15	I/O	COM		EVENTOUT	SEG5
								SPI2_MOSI/I^2S2_SD	
								TIM15_CH2	
								TIM1_CH3N	
								TIM15_CH1N	
37	-	-	-	PC6	I/O	COM		TIM3_CH1	SEG4
								SPI2_SCK/I^2S2_CK	
								USART4_RX	
								TIM2_CH3	
38	-	-	-	PC7	I/O	COM		TIM3_CH2	COMP3_INN4,

Packages				Reset	Port type	Port structure	Notes	Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K3					Alternate functions	Additional functions
								SPI2_MISO/I²S2_MCK	SEG3
								USART4_TX	
								TIM2_CH4	
39	-	-	-	PC8	I/O	COM		TIM3_CH3	SEG2
								SPI2_MOSI/I²S2_SD	
								USART4_CTS	
								TIM1_CH1	
40	-	-	-	PC9	I/O	COM		TIM3_CH4	SEG1
								SPI2_NSS/I²S2_WS	
								SPI1_SCK/I²S1_CK	
								USART4_RTS	
								TIM1_CH2	
41	29	29	18	PA8	I/O	COM		EVENTOUT	COM0, OPA1_OUT
								MCO	
								USART1_CK	
								TIM1_CH1	
								CTC_SYNC	
								SPI2_NSS	
								USART1_TX	
42	30	30	19	PA9	I/O	COM		EVENTOUT	COM1, OPA1_INP
								TIM15_BKIN	

Packages				Reset	Port type	Port structure	Notes	Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K3					Alternate functions	Additional functions
								USART1_TX	
								TIM1_CH2	
								I^2C1_SCL	
								SPI2_MISO/I^2S2_MCK	
								MCO	
								I^2C2_SCL	
43	31	31	20	PA10	I/O	COM		EVENTOUT	COM2, OPA1_INN
								TIM17_BKIN	
								USART1_RX	
								TIM1_CH3	
								I^2C1_SDA	
								SPI2_MOSI/I^2S2_SD	
								I^2C2_SDA	
44	32	32	21	PA11	I/O	COM_U		EVENTOUT	USB_DM, SEG0
								USART1_CTS	
								TIM1_CH4	
								CAN_RX	
								COMP1_OUT	
								SPI1_MISO/I^2S1_MCK	
								TIM1_BKIN2	
45	33	33	22	PA12	I/O	COM_U		EVENTOUT	USB_DP

Packages				Reset	Port type	Port structure	Notes	Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K3					Alternate functions	Additional functions
								USART1_RTS	
								TIM1_ETR	
								CAN_TX	
								COMP2_OUT	
								SPI1_MOSI/I²S1_SD	
								SPI1_SCK/I²S1_CK	
46	34	34	23	PA13-SWD	I/O	COM	(2)	EVENTOUT	-
								SWDIO	
								IR_OUT	
								USART1_RX	
								COMP3_OUT	
								PVD_OUT	
47	35	35	24	PF5	I/O	COM		TIM1_BKIN2	RTC_OUT, COM3
48	36	36	-	PF6	I/O	COM		USART1_CTS	-
49	37	37	25	PA14-SWC	I/O	COM	(2)	EVENTOUT	-
								SWCLK	
								USART2_TX	
								USART1_TX	
								PVD_OUT	
50	38	38	-	PA15	I/O	COM		EVENTOUT	-

Packages				Reset	Port type	Port structure	Notes	Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K3					Alternate functions	Additional functions
								SPI1_NSS/I²S1_WS	
								USART2_RX	
								TIM2_CH1_ETR	
								USART4_RTS	
								USART3_RTS	
51	-	-	-	PC10	I/O	COM		USART4_TX	COM4/SEG39
								USART3_TX	
								TIM1_CH3	
52	-	-	-	PC11	I/O	COM		USART4_RX	COM5/SEG38
								USART3_RX	
								TIM1_CH4	
53	-	-	-	PC12	I/O	COM		USART4_CK	COM6/SEG37
								USART3_CK	
								TIM14_CH1	
54	-	-	-	PF7	I/O	COM		TIM3_ETR	COM7/SEG36
								USART3_RTS	
								TIM1_CH1N	
55	39	39	-	PB3	I/O	COM		EVENTOUT	COMP2_INN9, SEG35/VLCDH
								SPI1_SCK/I²S1_CK	
								TIM2_CH2	
								USART1_RTS	

Packages				Reset	Port type	Port structure	Notes	Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K3					Alternate functions	Additional functions
								TIM1_CH2	
56	40	40	26	PB4	I/O	COM		EVENTOUT	COMP1_INP12, COMP2_INP12, SEG34/VLCD3
								SPI1_MISO/I²S1_MCK	
								TIM3_CH1	
								USART1_CTS	
								USART1_CK	
								TIM1_CH2N	
								TIM17_BKIN	
57	41	41	27	PB5	I/O	COM		SPI1_MOSI/I²S1_SD	COMP1_INP13, SEG33/VLCD2
								TIM3_CH2	
								TIM16_BKIN	
								I²C1_SMBA	
								USART1_CK	
								COMP2_OUT	
								USART1_RTS	
								USART1_TX	
								TIM1_CH3N	
58	42	42	28	PB6	I/O	COM		EVENTOUT	COMP1_INP14, COMP2_INP14, SEG32/VLCD1
								USART1_TX	
								I²C1_SCL	
								TIM16_CH1N	

Packages				Reset	Port type	Port structure	Notes	Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K3					Alternate functions	Additional functions
								SPI2_MISO/I²S2_MCK	
								USART3_CTS	
								TIM1_CH3	
								I²C2_SCL	
59	43	43	29	PB7	I/O	COM		EVENTOUT	PVD_IN, COMP2_INP15, SEG31
								USART1_RX	
								I²C1_SDA	
								TIM17_CH1N	
								USART4_CTS	
								SPI2_MOSI/I²S2_SD	
								I²C2_SDA	
								TIM1_CH1	
60	44	44	30	PF8/BOOT	I/O	COM	(3)		SEG30
61	45	45	31	PB8	I/O	COM		EVENTOUT	SEG29
								I²C1_SCL	
								I²C2_SCL	
								TIM16_CH1	
								SPI2_SCK/I²S2_CK	
								USART1_TX	
								USART3_TX	
								CAN_RX	

Packages				Reset	Port type	Port structure	Notes	Functions	
LQFP64 R1	LQFP48 C1	QFN48 C1	QFN32 K3					Alternate functions	Additional functions
								TIM15_BKIN	
								TIM1_CH1N	
62	46	46	32	PB9	I/O	COM		EVENTOUT	SEG28
								IR_OUT	
								I^2C1_SDA	
								TIM17_CH1	
								SPI2_NSS/I^2S2_WS	
								USART1_RX	
								USART3_RX	
								CAN_TX	
								I^2C2_SDA	
63	47	47	-	V_{SS}	G			Ground	
64	48	48	-	V_{CC}	S			Digital power supply	

1. Configured by option bytes to choose PF2 or NRST.
2. After reset, PA13 and PA14 are configured as SWDIO and SWCLK AF functions, the former has an internal pull-up resistor and the latter has an internal pull-down resistor activated.
3. PF8-BOOT0 defaults to digital input mode and pull-down is enabled.

3.1. Alternate functions selected through GPIOA_AFR registers for port A

Table 3-3 Port A alternate functions mapping

PortA	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	-	USART2_CTS	TIM2_CH1_ETR	-	USART4_TX	-	-	COMP1_OUT	SPI2_SCK	-	-	-	-	-	-	-
PA1	EVENTOUT	USART2_RTS	TIM2_CH2	-	USART4_RX	TIM15_CH1N	I²C1_SMBA	-	SPI1_SCK/ I²S1_CK	SPI2_MOSI	-	-	-	-	-	-
PA2	TIM15_CH1	USART2_TX	TIM2_CH3	-	-	-	-	COM2_OUT	SPI1_MOSI/ I²S1_SD	SPI2_MISO	-	-	-	-	-	-
PA3	TIM15_CH2	USART2_RX	TIM2_CH4	-	-		-	EVENTOUT	SPI2_MSIO	SPI2_NSS/ I²S2_WS	-	-	-	-	-	-
PA4	SPI1_NSS/ I²S1_WS	USART2_CK	-	-	TIM14_CH1	-	-	EVENTOUT	SPI2_MOSI	USART2_TX	-	-	PVD_OUT	-	-	-
PA5	SPI1_SCK/ I²S1_CK	-	TIM2_CH1_ETR	-	-	-	-	EVENTOUT	-	-	USART3_TX	-	-	-	-	-
PA6	SPI1_MISO/ I²S1_MCK	TIM3_CH1	TIM1_BKIN	-	USART3_CTS	TIM16_CH1	EVENTOUT	COMP1_OUT	-	-	-	-	-	-	-	-
PA7	SPI1_MOSI/ I²S1_SD	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT	-	-	-	-	-	-	-	-
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	CTC_SYNC	-	-	-	SPI2_NSS	-	USART1_TX	-	-	-	-	-
PA9	TIM15_BKIN	USART1_TX	TIM1_CH2	-	-	-	I²C1_SCL	EVENTOUT	SPI2_MISO	MCO	-	-	-	I²C2_SCL	-	-
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	-	-	-	I²C1_SDA	EVENTOUT	SPI2_MOSI	-	-	-	-	I²C2SDA	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	-	CAN_RX		-	COMP1_OUT	SPI1_MISO/ I²S1_MCK	-	-	TIM1_BKIN2	-	-	-	-
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	-	CAN_TX	-	-	COMP2_OUT	SPI1_MOSI/ I²S1_SD	I²S1_CKIN	-	-	-	-	-	-
PA13	SWDIO	IROUT	-	-	-	-	-	EVENTOUT	-	USART1_RX	-	COMP3_OUT	PVD_OUT	-	-	-
PA14	SWCLK	USART2_TX	-	-	-	-	-	EVENTOUT	-	USART1_TX	-	-	PVD_OUT	-	-	-
PA15	SPI1_NSS/ I²S1_WS	USART2_RX	TIM2_CH1_ETR	EVENTOUT	USART4_RTS			EVENTOUT			USART3_RTS					

3.2. Alternate functions selected through GPIOB_AFR registers for port B

Table 3-4 Port B alternate function mapping

PortB	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	-	USART3_CK	-	-	COMP1_OUT	SPI1_NSS/ I²S1_WS	-	USART3_RX	-	-	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	USART3_RTS	-	-	EVENTOUT	-	-	-	COMP3_OUT	-	-	-	-
PB2	-	-	-	-	-	-	-	EVENTOUT	SPI2_MISO	-	USART3_TX	-	-	-	-	-
PB3	SPI1_SCK/ I²S1_CK	EVEN-TOUT	TIM2_CH2	-	USART1_RTS	-	-	EVENTOUT	-	-	-	TIM1_CH2	-	-	-	-
PB4	SPI1_MISO/ I²S1_MCK	TIM3_CH1	EVENTOUT	-	USART1_CTS	TIM17_BKIN	-	-	-	-	-	TIM1_CH2N	-	USART1_CK	-	-
PB5	SPI1_MOSI/ I²S1_SD	Tim3_CH2	TIM16_BKIN	I²C1_SMBA	USART1_CK	-	-	COM2_OUT	-	USART1_RTS	-	TIM1_CH3N	-	USART1_TX	-	-
PB6	USART1_TX	I²C1_SCL	TIM16_CH1N	-	-	-	-	EVENTOUT	SPI2_MISO	-	USART3_CTS	TIM1_CH3	-	I²C2_SCL	-	-
PB7	USART1_RX	I²C1_SDA	TIM17_CH1N	-	USART4_CTS	-	-	EVENTOUT	SPI2_MOSI	-	-	TIM1_CH1	-	I²C2_SDA	-	-
PB8	-	I²C1_SCL	TIM16_CH1	-	CAN_RX	-	-	EVENTOUT	SPI2_SCK	USART1_TX	USART3_TX	TIM15_BKIN	-	I²C2_SCL	TIM1_CH1N	-
PB9	IR_OUT	I²C1_SDA	TIM17_CH1	EVENTOUT	CAN_TX	SPI2_NSS/ I²S2_WS	-	-	-	USART1_RX	USART3_RX	-	-	I²C2_SDA	-	-
PB10	-	I²C2_SCL	TIM2_CH3	-	USART3_TX	SPI2_SCK/ I²S2_CK	-	COMP1_OUT	-	USART2_RTS	-	-	-	I²C1_SCL	-	-
PB11	EVENTOUT	I²C2_SDA	TIM2_CH4	-	USART3_RX	-	-	COMP2_OUT	SPI2_MOSI	USART2_CTS	-	-	-	I²C1_SDA	-	-
PB12	SPI2_NSS/ I²S2_WS	EVEN-TOUT	TIM1_BKIN	-	USART3_CK	TIM15_BKIN	-	-	-	-	-	-	-	-	-	-
PB13	SPI2_SCK/ I²S2_CK	-	TIM1_CH1N	-	USART3_CTS	I²C2_SCL	-	EVENTOUT	-	MCO	-	TIM15_CH1N	-	I²C1_SCL	-	-
PB14	SPI2_MISO/ I²S2_MCK	TIM15_CH1	TIM1_CH2N	-	USART3_RTS	I²C2_SDA	-	EVENTOUT	-	-	-	-	-	I²C1_SDA	-	-
PB15	SPI2_MOSI/ I²S2_SD	TIM15_CH2	TIM1_CH3N	TIM15_CH1N	-	-	-	EVENTOUT	-	-	-	-	-	-	-	-

3.3. Alternate functions selected through GPIOC_AFR registers for port C

Table 3-5 Port C alternate function mapping

PortC	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0	EVENTOUT	-	-	-	-	-	-	-	SPI1_MISO/I²S1_MCK	USART2_CTS	USART3_RTS	-	-	-	-	-
PC1	EVENTOUT	-	-	-	-	-	-	-	SPI1_MOSI/I²S1_SD	USART2_RTS	USART3_CTS	TIM15_CH1	-	-	-	-
PC2	EVENTOUT	SPI2_MISO/I²S2_MCK	-	-	-	-	-	-	-	USART3_TX	USART3_RX	TIM15_CH2	-	-	-	-
PC3	EVENTOUT	SPI2_MOSI/I²S2_SD	-	-	-	-	-	-	-	USART3_RX	USART3_TX	-	-	-	-	-
PC4	EVENTOUT	USART3_TX	-	-	-	-	-	COMP3_OUT	SPI1_NSS/I²S1_WS	USART1_TX	-	TIM2_CH1_ETR	IR_OUT	-	-	-
PC5	-	USART3_RX	-	-	-	-	-	-	SPI1_MOSI/I²S1_SD	USART1_RX	-	TM2_CH2	-	-	-	-
PC6	TIM3_CH1	-	-	-	-	-	-	-	SPi2_SCK/I²S2_CK	-	USART4_RX	TIM2_CH3	-	-	-	-
PC7	TIM3_CH2	-	-	-	-	-	-	-	SPI2_MISO/I²S2_MCK	-	USART4_TX	TIM2_CH4	-	-	-	-
PC8	TIM3_CH3	-	-	-	-	-	-	-	SPI2_MOSI/I²S2_SD	-	USART4_CTS	TIM1_CH1	-	-	-	-
PC9	TIM3_CH4	-	-	-	-	-	-	-	SPI2_NSS/I²S2_WS	I²S1_CKIN	USART4_RTS	TIM1_CH2	-	-	-	-
PC10	USART4_TX	USART3_TX	-	-	-	-	-	-	-	-	-	TIM1_CH3	-	-	-	-
PC11	USART4_RX	USART3_RX	-	-	-	-	-	-	-	-	-	TIM1_CH4	-	-	-	-
PC12	USART4_CK	USART3_CK	-	-	-	-	-	-	-	-	-	TIM14_CH1	-	-	-	-
PC13	-	-	-	-	-	-	-	-	SPI1_SCK/I²S1_CK	-	-	TIM1_BKIN	-	-	-	-
PC14	-	-	-	-	-	-	-	-	-	-	-	TIM1_BKIN2	-	-	-	-
PC15	-	-	-	-	-	-	-	-	-	-	-	TIM15_BKIN	-	-	-	-

3.4. Alternate functions selected through GPIOF_AFR registers for port F

Table 3-7 Port F alternate function mapping

PortC	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0	EVENTOUT	-	-	-	-	-	-	-	SPI1_MISO/I2S1_MCK	USART2_CTS	USART3_RTS	-	-	-	-	-
PC1	EVENTOUT	-	-	-	-	-	-	-	SPI1_MOSI/I2S1_SD	USART2_RTS	USART3_CTS	TIM15_CH1	-	-	-	-
PC2	EVENTOUT	SPI2_MISO/I2S2_MCK	-	-	-	-	-	-	-	USART3_TX	USART3_RX	TIM15_CH2	-	-	-	-
PC3	EVENTOUT	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	-	USART3_RX	USART3_TX	-	-	-	-	-
PC4	EVENTOUT	USART3_TX	-	-	-	-	-	COMP3_OUT	SPI1_NSS/I2S1_WS	USART1_TX	-	TIM2_CH1_ETR	IR_OUT	-	-	-
PC5	-	USART3_RX	-	-	-	-	-	-	SPI1_MOSI/I2S1_SD	USART1_RX	-	TM2_CH2	-	-	-	-
PC6	TIM3_CH1	-	-	-	-	-	-	-	SPi2_SCK/I2S2_CK	-	USART4_RXD	TIM2_CH3	-	-	-	-
PC7	TIM3_CH2	-	-	-	-	-	-	-	SPI2_MISO/I2S2_MCK	-	USART4_TX	TIM2_CH4	-	-	-	-
PC8	TIM3_CH3	-	-	-	-	-	-	-	SPI2_MOSI/I2S2_SD	-	USART4_CTS	TIM1_CH1	-	-	-	-
PC9	TIM3_CH4	-	-	-	-	-	-	-	SPI2_NSS/I2S2_WS	I2S1_CKIN	USART4_RTS	TIM1_CH2	-	-	-	-
PC10	USART4_TX	USART3_TX	-	-	-	-	-	-	-	-	-	TIM1_CH3	-	-	-	-
PC11	USART4_RX	USART3_RX	-	-	-	-	-	-	-	-	-	TIM1_CH4	-	-	-	-
PC12	USART4_CK	USART3_CK	-	-	-	-	-	-	-	-	-	TIM14_CH1	-	-	-	-
PC13	-	-	-	-	-	-	-	-	SPI1_SCK/I2S1_CK	-	-	TIM1_BKIN	-	-	-	-
PC14	-	-	-	-	-	-	-	-	-	-	-	TIM1_BKIN2	-	-	-	-
PC15	-	-	-	-	-	-	-	-	-	-	-	TIM15_BKIN	-	-	-	-

4. Memory Mapping

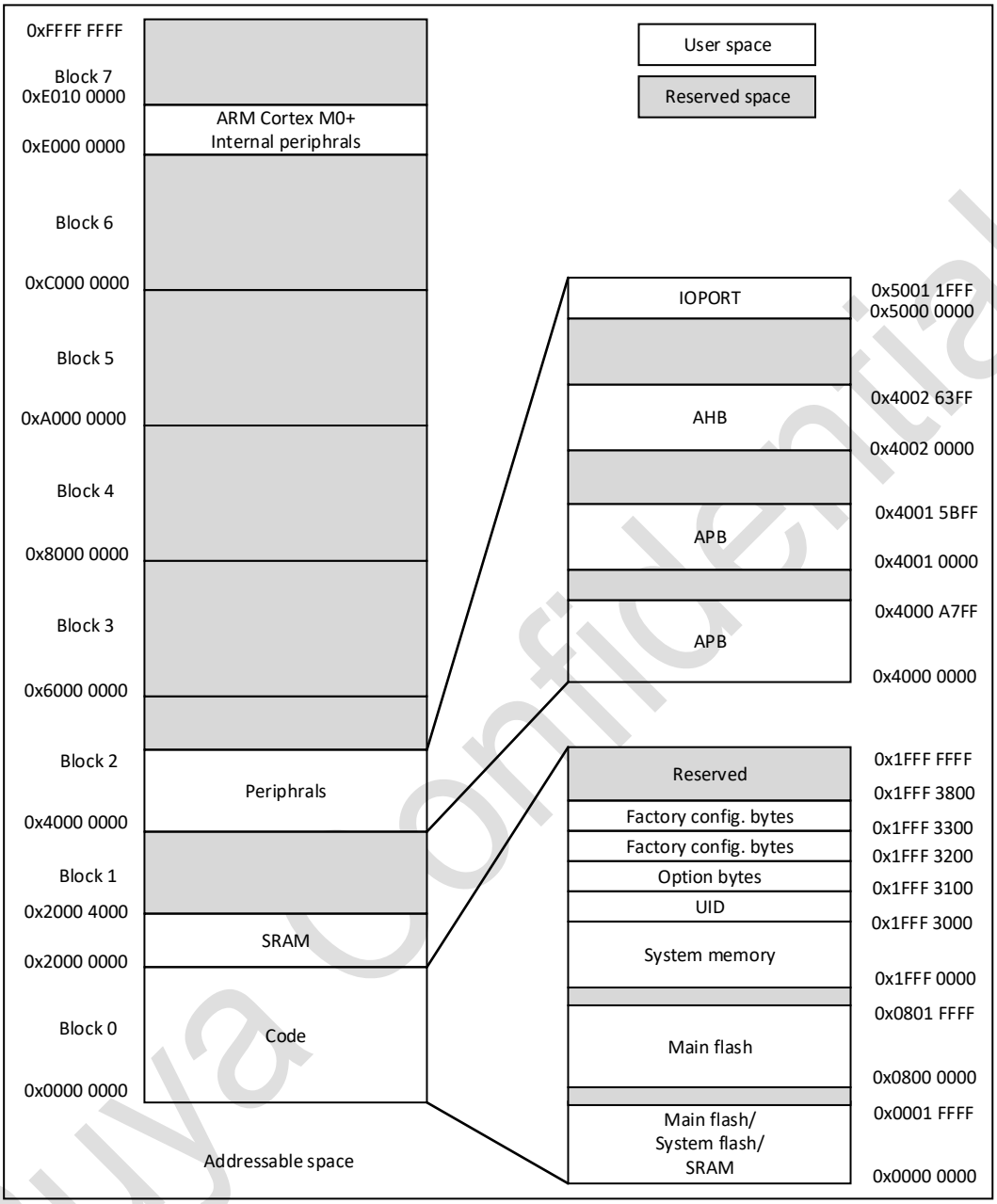


Table 4-1 Memory boundary address

Type	Boundary Address	Size	Memory Area	Description
SRAM	0x2000 4000-0x3FFF FFFF	-	Reserved(1)	-
	0x2000 0000-0x2000 3FFF	16 KB	SRAM	Up to 16 KB SRAM
Code	0x1FFF 3400-0x1FFF FFFF	-	Reserved	-
	0x1FFF 3300-0x1FFF 33FF	-	Reserved	Reserved
	0x1FFF 3200-0x1FFF 32FF	256 Bytes	FT info0 bytes	Factory config
	0x1FFF 3100-0x1FFF 31FF	256 Bytes	Option bytes	Option bytes information
	0x1FFF 3000-0x1FFF 30FF	256 Bytes	UID bytes	Unique ID
	0x1FFF 2F00-0x1FFF 2FFF	256 Bytes	FT bytes	FT bytes
	0x1FFF 0000-0x1FFF 2EFF	11.75 KB	System memory	Boot loader
	0x0802 0000-0x1FFE FFFF	-	Reserved	-
	0x0800 0000-0x0801 FFFF	128 KB	Main flash memory	-
	0x0002 0000-0x07FF FFFF	-	Reserved	-
	0x0000 0000-0x0001 FFFF	128 KB	Selected based on Boot configuration,: 1.Main flash memory 2.System memory 3.SRAM	-

1. The address is marked as Reserved , which cannot be written , read as 0 , and a response error is generated .

Table 4-2 Peripheral register boundary address(1)

Bus	Boundary Address	Size	Peripheral
	0xE000 000-0xE00F FFFF	1 MB	M0+
IOPORT	0x5000 1800 - 0x5FFF FFFF	-	Reserved
	0x5000 1400 - 0x5000 17FF	1 KB	GPIOF
	0x5000 1000 - 0x5000 13FF	1 KB	Reserved
	0x5000 0C00 - 0x5000 0FFF	1 KB	Reserved
	0x5000 0800 - 0x5000 0BFF	1 KB	GPIOC
	0x5000 0400 - 0x5000 07FF	1 KB	GPIOB
	0x5000 0000 - 0x5000 03FF	1 KB	GPIOA
AHB	0x4002 4000 - 0x4FFF FFFF	-	Reserved
	0x4002 3C00 – 0x4002 3FFF	-	Reserved
	0x4002 3800 –0x4002 3BFF	1 KB	DIV
	0x4002 3400 - 0x4002 37FF	1 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	-	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	Flash
	0x4002 1C00 - 0x4002 1FFF	-	Reserved
	0x4002 1800 - 0x4002 1BFF	1 KB	EXTI
	0x4002 1400 - 0x4002 17FF	-	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC(2)
	0x4002 0400 - 0x4002 0FFF	-	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA

Bus	Boundary Address	Size	Peripheral
APB	0x4001 5C00 - 0x4001 FFFF	-	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBG
	0x4001 4C00 - 0x4001 57FF	-	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	-	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	-	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	-	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0400 - 0x4001 23FF	-	Reserved
	0x4001 0300 - 0x4001 03FF	1 KB	OPA
	0x4001 0200 - 0x4001 02FF		COMP
	0x4001 0000 - 0x4001 01FF		SYSCFG
	0x4000 8000- 0x4000 FFFF	-	Reserved
	0x4000 7C00 - 0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800 - 0x4000 7BFF	-	Reserved
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR(3)
	0x4000 6C00 - 0x4000 6FFF	1 KB	CTC
	0x4000 6800 - 0x4000 6BFF	-	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	CAN
	0x4000 6000 - 0x4000 63FF	1 KB	USB SRAM
	0x4000 5C00 - 0x4000 5FFF	1 KB	USB
	0x4000 5800 - 0x4000 5BFF	1 KB	I^2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I^2C1
	0x4000 5000 - 0x4000 53FF	-	Reserved
	0x4000 4C00 - 0x4000 4FFF	1 KB	USART4
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 3C00 - 0x4000 43FF	-	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	LCD

Bus	Boundary Address	Size	Peripheral
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1800 - 0x4000 1FFF	-	Reserved
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0800 - 0x4000 0FFF	-	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

1. In the above table, the reserved address cannot be written, read back is 0, and a hardfault is generated
2. Support 32 bits word, half-word and byte access.
3. Support 32 bits word and half-word access.

5. Electrical Characteristics

5.1. Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1. Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A =25 °C and T_A =$T_{A(max)}$ (given by the selected temperature range).

Data based on electrical characterization results, design simulations and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization,the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation.

5.1.2. Typical values

Unless otherwise specified, typical data are based on T_A =25 °C and V_{CC} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated.

5.1.3. Power supply scheme

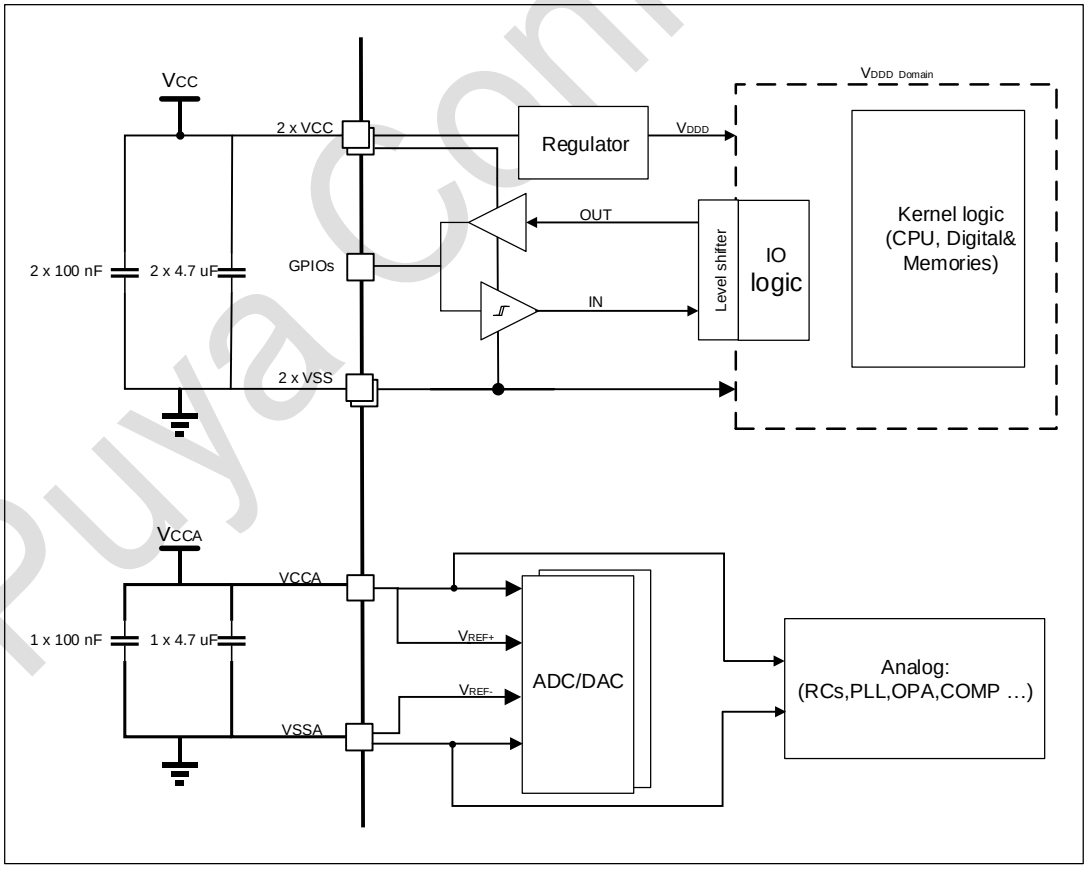


Figure 5-1 Power supply scheme

5.2. Absolute maximum ratings

Stresses above the absolute maximum ratings listed in following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5-1 Voltage characteristics (1)

Symbol	Ratings	Min	Max	Unit
V_{CC}–V_{SS}	External mains power supply	-0.3	6.25	V
V_{IN}	Input voltage of other pins	-0.3	V_{CC}+0.3	V

1. All main power (V_{CC},V_{CCA}) and ground (V_{SS},V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

Table 5-2 Current characteristics

Symbol(2)	Ratings	Max	Unit
ΣI_{VCC}	Total current into sum of all V_{CC} power lines (source)(1)	170	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink) (1)	170	mA
$I_{IO(PIN)}$ (2)	Output current sunk by any I/O and control pin	20	mA
	Output current source by any I/Os and control pin	20	
$\Sigma I_{IO(PIN)}$ (2)	Total output current sunk by sum of all I/Os and control pins	150	mA
	Total output current sourced by sum of all I/Os and control pins	150	

1. Power supply V_{CC} and ground V_{SS} pins must always be connected to the external power supply within the allowable range.

2. These I/O types refer to the terms and symbols defined by pins.

Table 5-3 Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
T_{STG}	Storage temperature range	-	-65 to +150	℃
T_O	Operating temperature range	-	-40 to +105	℃

5.3. Operating conditions

5.3.1. General operating conditions

Table 5-4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK}	Internal APB Clock frequency	-	0	72	MHz
V_{CC}	Standard operating voltage	-	1.7	5.5	V
V_{CCA}	Operating voltage of analog circuit	Must be the same as V_{CC} (1)	1.7	5.5	V
V_{IN}	I/O input voltage	-	-0.3	V_{CC}+0.3	V
T_A	Ambient temperature	-	-40	105	℃
T_J	Junction temperature	-	-40	110	℃

1. It is recommended to use the same power supply for V_{CC} and V_{CCA}, a maximum of 300 mV difference is allowed between V_{CC} and V_{CCA} during power-up and normal operation.

5.3.2. Operating conditions at power-up / power-down

Table 5-5 Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VCC}	V_{CC} rise time rate	-	0	∞	μs/V
	V_{CC} fall time rate	-	20	∞	

5.3.3. Embedded reset and PVD module characteristics

Table 5-6 POR/PDR/BOR module characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization	-	-	4.0	7.5	ms
$V_{POR/PDR}$	Power-on/power-off reset threshold	Rising edge	1.5	1.6	1.7	V
		Falling edge	1.45	1.55	1.65	
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	50	-	mV
V_{BOR}	BOR threshold	BOR_LEV[2:0]=000 (Rising edge)	1.7	1.8	1.9	V
		BOR_LEV[2:0]=000 (Falling edge)	1.6	1.7	1.8	
		BOR_LEV[2:0]=001 (Rising edge)	1.9	2	2.1	
		BOR_LEV[2:0]=001 (Falling edge)	1.8	1.9	2	
		BOR_LEV[2:0]=010 (Rising edge)	2.1	2.2	2.3	
		BOR_LEV[2:0]=010 (Falling edge)	2	2.1	2.2	
		BOR_LEV[2:0]=011 (Rising edge)	2.3	2.4	2.5	
		BOR_LEV[2:0]=011 (Falling edge)	2.2	2.3	2.4	
		BOR_LEV[2:0]=100 (Rising edge)	2.5	2.6	2.7	
		BOR_LEV[2:0]=100 (Falling edge)	2.4	2.5	2.6	
		BOR_LEV[2:0]=101 (Rising edge)	2.7	2.8	2.9	
		BOR_LEV[2:0]=101 (Falling edge)	2.6	2.7	2.8	
		BOR_LEV[2:0]=110 (Rising edge)	2.9	3	3.1	
		BOR_LEV[2:0]=110 (Falling edge)	2.8	2.9	3	
		BOR_LEV[2:0]=111 (Rising edge)	3.1	3.2	3.3	
		BOR_LEV[2:0]=111 (Falling edge)	3	3.1	3.2	
$V_{\_BOR\_hyst}$	BOR hysteresis	-	-	100	-	mV

1. Guaranteed by design, not tested in production.

Table 5-7 PVD module characteristics

符号	参数	条件	最小值	典型值	最大值	单位
V_{PVD}(2)	PVD threshold	PLS[2:0]=000 (Rising edge)	1.7	1.8	1.9	V
		PLS[2:0]=000 (Falling edge)	1.6	1.7	1.8	
		PLS[2:0]=001 (Rising edge)	1.9	2	2.1	
		PLS[2:0]=001 (Falling edge)	1.8	1.9	2	
		PLS[2:0]=010 (Rising edge)	2.1	2.2	2.3	
		PLS[2:0]=010 (Falling edge)	2	2.1	2.2	
		PLS[2:0]=011 (Rising edge)	2.3	2.4	2.5	
		PLS[2:0]=011 (Falling edge)	2.2	2.3	2.4	

符号	参数	条件	最小值	典型值	最大值	单位
		PLS[2:0]=100 (Rising edge)	2.5	2.6	2.7	
		PLS[2:0]=100 (Falling edge)	2.4	2.5	2.6	
		PLS[2:0]=101 (Rising edge)	2.7	2.8	2.9	
		PLS[2:0]=101 (Falling edge)	2.6	2.7	2.8	
		PLS[2:0]=110 (Rising edge)	2.9	3	3.1	
		PLS[2:0]=110 (Falling edge)	2.8	2.9	3	
		PLS[2:0]=111 (Rising edge)	3.1	3.2	3.3	
		PLS[2:0]=111 (Falling edge)	3	3.1	3.2	
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.4. Supply current characteristics

Table 5-8 Current consumption in Run mode

Symbol	Condition						Typ (1)	Max (1)		Unit
	System clock	Frequency	Code	Run	Peripheral clock	Flash sleep		T_A= 85 ℃	T_A= 105 ℃	
I_{CC}(Run)	PLL*3 PLL*2	72 MHz	While(1)	Flash	ON	DISABLE	8.4	10.7	14.4	mA
					OFF	DISABLE	4.6	5.3	6.3	
		48 MHz			ON	DISABLE	6.5	8.0	10.3	
					OFF	DISABLE	4.0	4.5	5.5	
	HSI	24 MHz			ON	DISABLE	3.8	4.3	5.3	
					OFF	DISABLE	2.6	2.8	3.8	
		16 MHz			ON	DISABLE	2.8	3.8	5.0	
					OFF	DISABLE	1.9	2.7	3.1	
		8 MHz			ON	DISABLE	1.8	2.5	3.1	
					OFF	DISABLE	1.2	2.3	3.0	
		4 MHz			ON	DISABLE	1.0	2.3	3.0	
					OFF	DISABLE	0.9	1.3	3.0	
	LSI	32.768 kHz			ON	DISABLE	0.4	0.6	1.1	
					OFF	DISABLE	0.3	0.5	0.9	
		32.768 kHz			ON	ENABLE	0.3	0.5	0.8	
					OFF	ENABLE	0.2	0.4	0.6	

1. Data based on characterization results, not tested in production.

Table 5-9 Current consumption in Sleep mode

Symbol	Condition				Typ(1)	Max (1)		Unit
	System clock	Frequency	Peripheral clock	Flash sleep		T_A=85 ℃	T_A=105 ℃	
I_{CC} (Sleep)	PLL*3 PLL*2	72 MHz	ON	DISABLE	6.2	8.2	11.2	mA
			OFF	DISABLE	2.1	2.7	3.8	
		48 MHz	ON	DISABLE	4.6	6.1	7.4	
			OFF	DISABLE	1.8	2.3	3.0	

Symbol	Condition				Typ(1)	Max (1)		Unit
	System clock	Frequency	Peripheral clock	Flash sleep		T_A=85 ℃	T_A=105 ℃	
	HSI	24 MHz	ON	DISABLE	2.1	2.9	3.8	
			OFF	DISABLE	0.9	1.2	1.7	
		16 MHz	ON	DISABLE	1.6	2.3	3.0	
			OFF	DISABLE	0.7	1.0	1.5	
		8 MHz	ON	DISABLE	1.0	2.3	3.0	
			OFF	DISABLE	0.5	0.8	1.3	
		4 MHz	ON	DISABLE	0.7	1.1	1.7	
			OFF	DISABLE	0.5	0.7	1.2	
	LSI	32.768 kHz	ON	DISABLE	0.3	0.6	1.1	
			OFF	DISABLE	0.3	0.5	0.9	
		32.768 kHz	ON	ENABLE	0.3	0.6	0.9	
			OFF	ENABLE	0.2	0.4	0.7	

1. Data based on characterization results, not tested in production.

Table 5-10 Current consumption in Stop mode

Symbol	Conditions					Typ (1)	Max		Unit
	V_{CC}	V_{DDx}	MR/LPR	LSI	Peripheral clock		T_A= 85 ℃	T_A= 105 ℃	
I_{CC}(Stop)	1.7 ~ 5.5 V	1.2 V	MR	-	-	130	356.7	519.1	μA
		1.2 V	LPR	ON	RTC + IWDG + LPTIM	9.2	212.2	330.5	
					IWDG	9.3	212.1	330.6	
					LPTIM	9.3	211.8	330.0	
					RTC	9.2	211.8	330.2	
				OFF	-	9.0	211.8	330.1	
		1.0 V		ON	RTC + IWDG + LPTIM	7.2	162.1	254.1	
					IWDG	7.3	162.1	254.0	
					LPTIM	7.3	161.8	253.7	
					RTC	7.2	161.8	253.5	
				OFF	-	7.0	161.8	253.6	
		0.9V		ON	RTC + IWDG + LPTIM	6.2	124.9	196.0	
					IWDG	6.3	124.9	196.1	
					LPTIM	6.3	124.6	195.5	
					RTC	6.2	124.6	195.6	
				OFF	-	6.0	124.6	195.6	
		0.8 V		ON	RTC + IWDG + LPTIM	5.2	110.8	233.9	
					IWDG	5.3	112.5	248.1	
					LPTIM	5.3	110.6	238.2	
					RTC	5.2	112.0	266.8	
				OFF	-	5.0	110.1	267.2	

1. Data based on characterization results, not tested in production.

5.3.5. Wakeup time from low-power mode

Table 5-11 Low-power mode wakeup timings

Symbol	Parameter(1)		Conditions	Typ (2)	Max	Unit
$t_{WUSLEEP}$	Wake-up from Sleep mode		-	7	-	CPU Cycles
t_{WUSTOP}	Wake-up from Stop mode	Regulator in Run mode(VR in MR mode)	Execute program in Flash, HSI (24 MHz) as system clock	3	-	μs
			Execute program in Flash, HSI (8 MHz) as system clock	4.5	-	
		Regulator in Low power mode (VR in LPR mode)	Execute program in Flash, HSI (24 MHz) as system clock	6	-	
			Execute program in Flash, HSI (8 MHz) as system clock	7	-	

1. The wake-up time is measured from the wake-up time until the first instruction is read by the user program.
2. Data based on characterization results, not tested in production.

5.3.6. External clock source characteristics

5.3.6.1. High-speed external clock generated from an external source

In bypass mode of HSE (the HSEBYP of RCC_CR is set), when the high-speed start-up circuit in the chip stops working, the corresponding I/O is used as a standard GPIO.

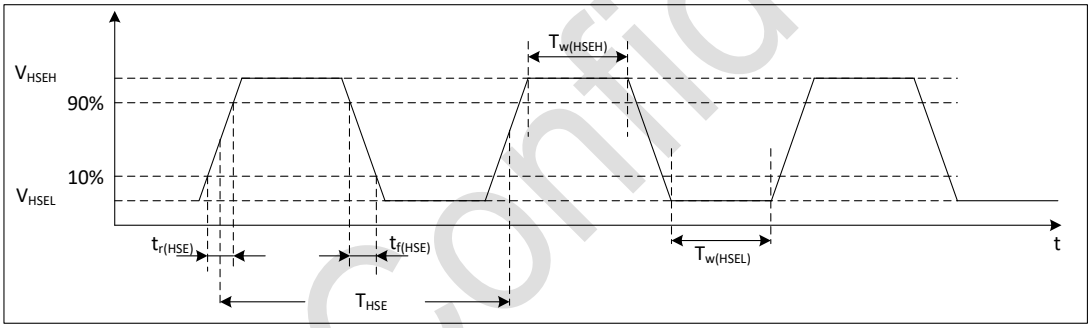


Figure 5-2 High-speed external clock timing diagram

Table 5-12 High-speed external clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	1	8	32	MHz
V_{HSEH}	Input pin high level voltage	$0.7V_{CC}$	-	V_{CC}	V
V_{HSEL}	Input pin low level voltage	V_{SS}	-	$0.3V_{CC}$	
$t_{W(HSEH)}$ $t_{W(HSEL)}$	High or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	Rise or fall time	-	-	20	ns

1. Guaranteed by design, not tested in production.

5.3.6.2. Low-speed external clock generated from an external source

In the bypass mode of LSE (the LSE BYP of RCC_BDCR is set), the low-speed start-up circuit in the chip stops working, and the corresponding I/O is used as a standard GPIO.

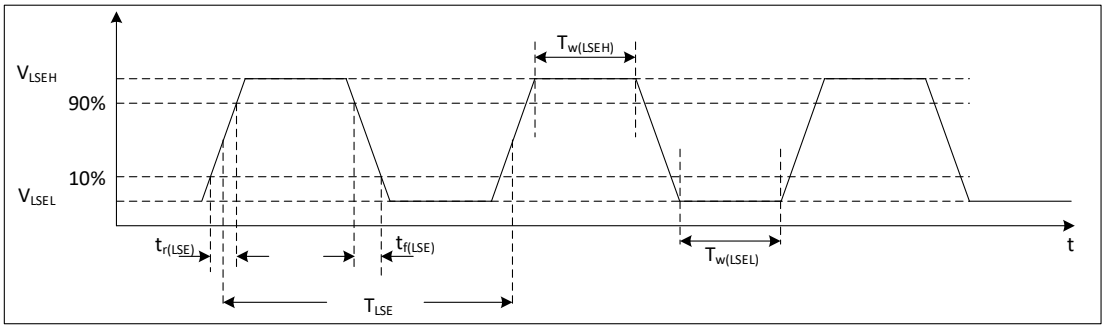


Figure 5-3 Low-speed external clock timing diagram

Table 5-13 Low-speed external clock characteristics

Symbol	Parameter[1]	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock frequency	-	32.768	1000	kHz
V_{LSEH}	Input pin high level voltage	$0.7V_{CC}$	-	-	V
V_{LSEL}	Input pin low level voltage	-	-	$0.3V_{CC}$	V
$t_{W(LSEH)}$ $t_{W(LSEL)}$	High or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	Rise or fall time	-	-	50	ns

1. Guaranteed by design, not tested in production.

5.3.6.3. High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with 4 ~ 32 MHz crystal/ceramic resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-14 HSE oscillator characteristics

Symbol	Parameter	Conditions[1]	Min [2]	Typ	Max [2]	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	32	MHz
I_{CC}[4]	HSE current consumption	During startup	-	-	5.5	mA
		V_{CC}=3 V,R_m=80 Ω, C_L=20 pF@ 8 MHz HSE_DRV [1:0] = 01	-	0.45	-	
		V_{CC}=3 V,R_m=80 Ω, CL=20 pF@ 16 MHz HSE_DRV [1:0] = 10	-	1.00	-	
		V_{CC}=3 V,R_m=30 Ω, C_L=20 pF@ 24 MHz HSE_DRV [1:0] = 10	-	1.10	-	
		V_{CC}=3 V,R_m=30 Ω, C_L=20 pF@ 24 MHz HSE_DRV [1:0] = 11	-	1.40	-	
		V_{CC}=3 V,R_m=35 Ω, C_L=20 pF@ 32 MHz HSE_DRV [1:0] = 11	-	1.50	-	
$t_{SU(HSE)}$[3] [4]	Startup time	f_{OSC_IN}= 4 MHz,R_m=100 Ω, C_L=12 pF@ 4MHz HSE_STARTUP [1:0] = 00 HSE_DRV [1:0] = 01	-	1.8	-	ms
		f_{OSC_IN}= 32 MHz,Rm=35 Ω, C_L=20 pF@ 32 MHz	-	2	-	

Symbol	Parameter	Conditions[1]	Min [2]	Typ	Max [2]	Unit
		HSE_STARTUP [1:0] = 00 HSE_DRV [1:0] = 11				

1. Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.
2. Guaranteed by design, not tested in production.
3. $t_{SU(HSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable state , measured for a standard crystal/resonator, which can vary considerably from one crystal/resonator to another .
4. Data based on characterization results, not tested in production.

5.3.6.4. Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 5-15 LSE oscillator characteristics

Symbol	Parameter	Conditions[1]	Min [2]	Typ	Max [2]	Unit
I_{CC}[4]	LSE current consumption	C_L=6 pF@ 32.768 kHz LSE_DRIVER [1:0] = 01	-	0.7	-	µA
		C_L=12 pF@ 32.768 kHz LSE_DRIVER [1:0] = 10	-	1.1	-	
		C_L=12 pF@ 32.768 kHz LSE_DRIVER [1:0] = 11	-	1.3	-	
$t_{SU(LSE)}$[3][4]	Startup Time	LSE_STARTUP [1:0] = 00	-	3	-	s

1. Crystal/ceramic resonator characteristics are based on the manufacturer's datasheet.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time from enable (by software) to when the clock oscillation reaches a stable , measured for a standard crystal/resonator , which may vary greatly from crystal to resonator.
4. Data based on characterization results, not tested in production.

5.3.7. High-speed internal (HSI) RC oscillator

Table 5-16 HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI frequency	-	-	4.0 8.0 16.0 22.12 24.0	-	MHz
$\Delta_{Temp(HSI)}$	HSI frequency drift over temperature	V_{CC} = 1.7 to 5.5 V, T_A = 25 °C	-1[2]	-	1[2]	%
		V_{CC} = 1.7 to 5.5 V, T_A = 0 to 85 °C	-2[2]	-	2[2]	
		V_{CC} = 1.7 to 5.5 V, T_A = -40 to 85 °C	-4[2]	-	2[2]	
		V_{CC} = 1.7 to 5.5 V, T_A = -40 to 105 °C	-4[2]	-	4[2]	
D_{HSI}[1]	Duty cycle	-	45[1]	-	55[1]	%
$t_{Stab(HSI)}$	HSI stabilization time	-	-	2	4[1]	µs
$I_{CC(HSI)}$ [2]	HSI power consumption	4 MHz	-	110	-	µA
		8 MHz	-	120	-	
		16 MHz	-	170	-	
		22.12 MHz, 24 MHz	-	210	-	

1. Guaranteed by design, not tested in production.

2. Data based on characterization results, not tested in production.

5.3.8. Low-speed internal (LSI) RC oscillator

Table 5-17 LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	-	-	32.768	-	kHz
$\Delta T_{emp(LSI)}$	LSI frequency drift over temperature	V_{CC} = 3.3 V,T_A = 25 °C	-3	-	+3	%
		V_{CC} = 1.7 ~ 5.5 V,T_A = 0 ~ 85 °C	-10(2)	-	10(2)	
		V_{CC}=1.7 ~ 5.5 V,T_A= 0 ~105 °C	- 15(2)	-	15(2)	
		V_{CC} = 1.7 ~ 5.5 V, T_A = -40 ~ 105 °C	-20(2)	-	20(2)	
$t_{Stab(LSI)}$(1)	LSI stabilization time	-	-	150	-	μs
$I_{CC(LSI)}$(1)	LSI power consumption	-	-	300	-	nA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.9. Phase locked loop (PLL) characteristics

Table 5-18 PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL Input clock	T_A = 25 °C, V_{CC} = 3.3 V PLL * 2	16(1)	-	24(1)	MHz
		T_A = 25 °C, V_{CC} = 3.3 V PLL * 3	22.12(1)	-	24(1)	
f_{PLL_OUT}	PLL output clock	T_A = 25 °C, V_{CC} = 3.3 V	32(1)	-	72	MHz
Jitter	Cycle-to-cycle jitter	-	-	-	0.3(1)	ns
t_{LOCK}	PLL lock time	f_{PLL_IN} = 24 MHz	-	15	40(1)	μs

1. Guaranteed by design, not tested in production.

5.3.10. Memory characteristics

Table 5-19 Memory characteristics

Symbol	Parameter	Conditions	Typ	Max (1)	Unit
t_{prog}	Page programming time	-	1.0	1.5	ms
t_{ERASE}	Page/sector/mass erase time	-	3.0	4.5	ms
I_{CC}	Page programming supply current	-	2.1	2.9	mA
	Page/sector/mass erase supply current	-	2.1	2.9	mA

1. Guaranteed by design, not tested in production.

Table 5-20 Memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = -40 ~ 85 ℃	100	kcycle
		T_A = 85 ~ 105 ℃	10	
t_{RET}	Data retention	10 kcycle T_A = 55 ℃	20	Year

1. Data is based on assessment results and is not tested in production.

5.3.11. EFT characteristics

Table 5-21 EFT characteristics(1)

Symbol	Parameter	Conditions	Level/Class
EFT to Power	-	IEC61000-4-4	4A

1. Data based on characterization results, not tested in production.

5.3.12. ESD & LU characteristics

Table 5-22 ESD & LU characteristics(1)

Symbol	Parameter	Conditions	Typ	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage(human body model)	ESDA/JEDEC JS-001-2017	6	kV
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	ESDA/JEDEC JS-002-2018	1	kV
LU	Static latch-up	JESD78E	200	mA

1. Data based on characterization results, not tested in production.

5.3.13. I/O port characteristics

Table 5-23 I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level input voltage	V_{CC} = 1.7 to 5.5 V	0.7V_{CC}	-	-	V
V_{IL}	Low level input voltage	V_{CC} = 1.7 to 5.5 V	-	-	0.3V_{CC}	V
V_{hys}(1)	Schmitt trigger hysteresis	-	-	200		mV
I_{lkg}	Input leakage current	-	-	-	1	µA
R_{PU}	Weak pull-up equivalent resistor	-	30	50	70	kΩ
R_{PD}	Weak pull-down equivalent resistor	-	30	50	70	kΩ
C_{IO}(1)	Pin capacitance	-	-	5	-	pF
$t_{ns(EXTI)}$ (1)	Input filter width	ENI=1, ENS=1	3	5	10	ns
$t_{ns(I2C)}$ (1)	I^2C Input filter width	ENI=1, EIIC=1	50	140	250	ns

1. Guaranteed by design, not tested in production.

Table 5-24 Output voltage characteristics

Symbol	Parameters(1)	Conditions		Min	Max	Unit
V_{OL}(2)	Output low level voltage for an I/O pin	GPIOx_OSPEEDR=11	I_{OL} = 8 mA, V_{CC} ≥ 2.7 V	-	0.4	V
			I_{OL} = 4 mA, V_{CC} = 1.8 V	-	0.5	
V_{OH}(2)	Output high level voltage for an I/O pin	GPIOx_OSPEEDR=11	I_{OH} = 8 mA, V_{CC} ≥ 2.7 V	V_{CC} - 0.4	-	V
			I_{OH} = 4 mA, V_{CC} = 1.8 V	V_{CC} - 0.5	-	

1. IO types can refer to the terms and symbols defined by the pins.
2. Data based on characterization results,not tested in production.
3. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in Table 5-2 Current characteristics, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.

5.3.14. ADC characteristics

Table 5-25 ADC characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	Analog supply voltage for ADC ON	-	1.8	-	5.5	V
V_{REF+}	Positive reference voltage	V_{REF+}= V_{CCA}	V_{CCA}			V
		V_{REF+}= V_{REFBUF}	-	1.5	-	
			-	2.048	-	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
			-	2.5	-	
V_{REF-}	Negative reference voltage	-		0		V
I_{VCCA}	ADC consumption from V_{CCA}	f_s=1 Msps	-	350	-	μA
I_{VREF+}	ADC consumption from V_{REF+}	f_s=1 Msps	-	22	-	μA
C_{ADC}(1)	Internal sample and hold capacitors	-	-	5	8	pF
R_{AIN}(1) (3)	External input impedance	-	-	-	31	kΩ
R_{ADC}(1)	Sampling switch resistance	-	-	-	2.5	kΩ
f_{ADC}	ADC clock frequency	V_{CCA}=1.8 ~ 2.3 V	0.8	4	8(2)	MHz
		V_{CCA}=2.3 ~ 5.5 V	0.8	8	16(2)	
f_S	Sampling rate	V_{CCA}=1.8 ~ 2.3 V	0.05	-	0.5	Msps
		V_{CCA}=2.3 ~ 5.5 V	0.05	-	1	
t_{CAL}(1)	Calibration time	f_{ADC} = 16 MHz	4.375	-	7.4375	μs
			70	-	119	$1/f_{ADC}$
t_{samp}(1)	Sampling time	f_{ADC}=16 MHz V_{CCA}=1.8 ~ 5.5 V	0.219	-	14.97	μs
			3.5	-	239.5	$1/f_{ADC}$
t_{samp_int}(1)	Sampling time for internal channels (V_{REFINT},T_{S_VIN},V_{CCA}/3,OPA 1~3,DAC 1~2)	-	15	-	-	μs
t_{conv}(1)	Total conversion time	V_{CCA}=1.8 ~ 5.5 V	12	-	248	$1/f_{ADC}$
t_{eoc}(1)	Conversion end time	V_{CCA}=1.8 ~ 5.5 V		0.5		$1/f_{ADC}$

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.
3. Equation 1: R_{AIN} max formula
4. $$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

   The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 5-26 R_{AIN} max for f_{ADC}=16 MHz(1)

Ts (cycles)	t_S (μs)	R_{AIN} max (kΩ)
3.5	0.21	0.3
5.5	0.34	1.9
7.5	0.46	3.5
13.5	0.84	8.3
28.5	1.78	20.4
41.5	2.59	30.9
134.5	8.41	-
239.5	14.96	-

1. Guaranteed by design, not tested in production.

Table 5-27 ADC accuracy(1)(2)

Symbol	Parameter	Conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{ADC} = 16 MHz, V_{CCA} = 1.8 V to 5.5 V	± 6.5	±10.0	LSB
EO	Offset error		± 1.3	± 3.0	LSB
EG	Gain error		± 2.6	± 5.0	LSB
DNL	Differential linearity error		± 1.2	± 1.5	LSB

Symbol	Parameter	Conditions	Typ	Max	Unit
INL	Integral linearity error		± 3.5	± 6.5	LSB

1. ADC DC accuracy values are measured after internal calibration.
2. Data based on characterization results,not tested in production.

5.3.15. DAC characteristics

Table 5-28 DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	Analog supply voltage for DAC ON	Buffer ON	2.2	-	5.5	V
		Buffer OFF	2.2	-	5.5	
R_{LOAD}(1)	Resistive load with buffer ON	Load connected to V_{SSA}	5	-	-	kΩ
		Load connected to V_{CCA}	15	-	-	
R_O(1)	Impedance output with buffer OFF	The minimum resistive load between DAC_VOUT and V_{SSA} to have a 1% accuracy is 1.5 MΩ(When the buffer is ON) .	-	-	15	kΩ
C_{LOAD}(1)	Capacitive load	Maximum capacitive load at DAC_OUT pin (When the buffer is ON).	-	-	50	pF
DAC_OUT min(1)	Lower DAC_OUT voltage	Buffer ON,it gives the maximum output excursion of the DAC.	0.2	-	-	V
DAC_OUT max(1)	Higher DAC_OUT voltage		-	-	V_{CCA} - 0.2	V
DAC_OUT min(1)	Lower DAC_OUT voltage	Buffer OFF,it gives the maximum output excursion of the DAC.	-	0.5	-	mV
DAC_OUT max(1)	Higher DAC_OUT voltage		-	-	V_{CCA} – 10 mV	V
I_{CCA}(1)	DAC DC current consumption in quiescent mode (2)	With no load, middle code (0x800) on the inputs	-	-	900	μA
		With no load, worst code (0xF1C) at V_{CCA} = 3.6 V in terms of DC consumption on the inputs	-	-	1200	
DNL(2)	Differential linearity error	Given for the DAC in 10 bits configuration	-	-	±1	LSB
		Given for the DAC in 12 bits configuration	-	-	±3	
INL(2)	Integral linearity error	Given for the DAC in 10 bits configuration	-	-	±1	LSB
		Given for the DAC in 12 bits configuration			±4	
Offset(2)	Offset error	Given for the DAC in 10 bits	-	-	±3	LSB
		Given for the DAC in 12 bits	-	-	±12	
Gain error(2)	Gain error	Given for the DAC in 12 bits configuration	-	-	±0.5	%
$t_{SETTLING}$(2)	Settling time	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ Full scale: for a 10 bits input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	4	10	μs
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ	-	-	1	MS/s
t_{WAKEUP}(2)	Wake-up time from off state	C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ Input code between lowest and highest possible ones.	-	6.5	10	μs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_{SRR+}(1)	Power supply rejection ratio (to V_{CCA}) (static DC measurement	No R_{LOAD} , C_{LOAD} = 50 pF	-	-67	-40	dB

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

5.3.16. Comparator characteristics

Table 5-29 Comparator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Input voltage range	-		0	-	V_{CCA}	V
V_{SC}	Scaler offset voltage	-		-	±5	± 10	mV
$I_{CCA(SCALER)}$	Scaler static consumption	-		-	0.8	1	μA
t_{START_SCALER}	Scaler startup time	-		-	100	200	μs
t_{START}	Startup time	High-speed mode		-	-	5	μs
		Medium-speed mode		-	-	15	
t_D	Propagation delay	200 mV step, 100 mV over-drive	High-speed mode	-	50	150	ns
			Medium-speed mode	-	1500	2800	
		>200 mV step, 100 mV over-drive	High-speed mode	-	-	200	
			Medium-speed mode	-	-	2900	
V_{offset}	Offset error	-		-	±5	± 10	mV
V_{hys}	Hysteresis voltage	No hysteresis		-	0	-	mV
		With hysteresis		-	20	-	
I_{CCA}	Consumption	Static	High-speed mode	-	250	-	μA
			Medium-speed mode	-	7	-	
		With 50 kHz and ±100 mv overdrive square signal	High-speed mode	-	250	-	
			Medium-speed mode	-	8	-	

1. Guaranteed by design, not tested in production.

5.3.17. Operational amplifier characteristics

Table 5-30 OPA characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	Analog supply voltage		2.2	-	5.5	V
V_{IN}	Input voltage	-	0	-	V_{CCA}	V
V_{OUT}	Output voltage	-	0.1	-	V_{CCA} - 0.2	V
I_{LOAD}	Drive current	-	-	-	2.2	mA
R_L	Resister load	-	5	-	-	kΩ
t_{start}	Initialization time	$C_{LOAD} \leqslant$ 50 pF, $R_{LOAD} \geqslant$ 5 kΩ	-	-	20	μs
V_{IO}	Input offset voltage	$C_{LOAD} \leqslant$ 50 pF, $R_{LOAD} \geqslant$ 5 kΩ Vcom=V_{CCA}/2	--	±6	-	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PM	Phase margin	C_{LOAD} ⩽ 50 pF, R_{LOAD} ⩾ 5 kΩ Vcom=V_{CCA}/2	-	80	-	Deg
UGBW	Unit Gain Bandwidth	C_{LOAD} ⩽ 50 pF, R_{LOAD} ⩾ 5 kΩ Vcom=V_{CCA}/2	-	10	-	MHz
SR	Slew rate	-	-	7	-	V/μs

5.3.18. Temperature sensor characteristics

Table 5-31 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	℃
Avg_Slope(1)	Average slope	2.3	2.5	2.7	mV/℃
V_{25}	Voltage at 25 ℃ (±5 ℃)	0.742	0.76	0.785	V
t_{START}(1)	Start up time entering in continuous mode	-	70	120	μs
t_{s_setup}(1)	ADC sampling time when reading the temperature	15	-	-	μs

1. Guaranteed by design, not tested in production.
2. Data is based on assessment results and is not tested in production.

5.3.19. LCD Controller Characteristics

Table 5-32 LCD Controller Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LCD}(1)(3)	LCD supply current	External drive resistive mode	-	0.6	-	μA
		Internal low drive resistive mode	-	4	-	
		Internal middle drive resistive mode	-	7.5	-	
		Internal high drive resistive mode	-	10	-	
R_H(2)	Low drive resistive	-	-	1080	-	kΩ
R_M(2)	Middle drive resistive	-	-	540	-	
R_L(2)	High drive resistive	-	-	360	-	
V_{LCDH}	LCD adjustable highest level voltage	-	-	V_{CCA}	-	V
V_{LCD3}	LCD highest level voltage	-	-	V_{LCDH}	-	
V_{LCD2}	LCD 2/3 level voltage	-	-	2/3 V_{LCDH}	-	
V_{LCD1}	LCD 1/3 level voltage	-	-	1/3 V_{LCDH}	-	
V_{LCD0}	LCD lowest level voltage	-	-	V_{SS}	-	
ΔV_{LCD}(3)	LCD segment/common level voltage error	T_A = -40 ~ 105 °C	-	-	±50	mV

1. LCD enabled with V_{CCA}=3.3 V, 1/4 duty, 1/3 bias,scan frequency 256 Hz, all pixels active, no LCD connected.
2. Guaranteed by design, not tested in production.
3. Data is based on assessment results and is not tested in production.

5.3.20. Embedded voltage reference characteristics

Table 5-33 Embedded internal voltage reference (V_{REFBUF}) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-	1.17	1.2	1.23	V
$t_{start\_VREFINT}$	Start time of V_{REFINT}	-	-	10	15	μs
$T_{coeff\_VREFINT}$	Temperature coefficient of V_{REFINT}	-	-	-	100(1)	ppm/℃
I_{vcc}	Current consumption from V_{CC}	-	-	12	20	μA

1. Guaranteed by design, not tested in production.

5.3.21. ADC voltage reference buffer characteristics

Table 5-34 ADC voltage reference buffer (V_{REFBUF}) characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFBUF25}$	2.5 V Internal reference voltage	T_A=25 °C,V_{CCA}=3.3 V	2.48	2.5	2.53	V
$V_{REFBUF20}$	2.048 V Internal reference voltage	T_A=25 °C,V_{CCA}=3.3 V	2.03	2.048	2.07	V
$V_{REFBUF15}$	1.5 V Internal reference voltage	T_A=25 °C,V_{CCA}=3.3 V	1.49	1.5	1.51	V
$t_{start\_VREFBUF}$	Start time of V_{REFBUF}	-	-	-	2	μs
$T_{coefft\_VREFBUF}$	Current consumption from V_{REFBUF}	T_A=-40 ~ 105 °C	-	-	120	ppm/°C

1. Guaranteed by design, not tested in production.

5.3.22. Timer characteristics

Table 5-35 Timer characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.889	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 72 MHz	-	24	
Res_{TIM}	Timer resolution	TIM1/3/14/15/16/17	-	16	bit
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.013889	913	μs

Table 5-36 LPTIM characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PRESC[2:0]	Min overflow	Max overflow	Unit
/1	0	0.0305	1998.848	ms
/2	1	0.0610	3997.696	
/4	2	0.1221	8001.9456	
/8	3	0.2441	15997.3376	
/16	4	0.4883	32001.2288	
/32	5	0.9766	64002.4576	
/64	6	1.9531	127998.3616	
/128	7	3.9063	256003.2768	

Table 5-37 IWDG characteristics (timeout period at 32.768 kHz LSI)

Prescaler	PR[2:0]	Min overflow	Max overflow	Unit
/4	0	0.122	499.712	ms
/8	1	0.244	999.424	
/16	2	0.488	1998.848	
/32	3	0.976	3997.696	
/64	4	1.952	7995.392	
/128	5	3.904	15990.784	
/256	6 or 7	7.808	31981.568	

Table 5-38 WWDG characteristics (timeout period at 48 MHz PCLK)

Prescaler	WDGTB[1:0]	Min overflow	Max overflow	Unit
1*4096	0	0.085	5.461	ms
2*4096	1	0.171	10.923	
4*4096	2	0.341	21.845	
8*4096	3	0.683	43.691	

5.3.23. Communication interfaces

5.3.23.1. I²C interface characteristics

The I²C interface meets the timing requirements of the I²C-bus specification and user manual:

- Standard-mode (Sm): up to100 kbit/s
- Fast-mode (Fm): up to 400 kbit/s

I²C SDA and SCL pins have analogue filtering, see table below.

Table 5-39 I²C filter characteristics

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum width of spikes that are suppressed by the analog filter	50	260	ns

5.3.23.2. SPI characteristics

Table 5-40 SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	24	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	2 T_{pclk}	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2 T_{pclk}	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, presc = 2	T_{pclk} - 2	T_{pclk} + 1	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	1	-	ns
		Slave mode	3	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	ns
$t_{h(SI)}$		Slave mode	2	-	
$t_{a(SO)}$	Data output access time	Slave mode	0	3 T_{pclk}	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	2 T_{pclk}	-	ns
$t_{v(SO)}$	Data output valid time	Slave mode(after enable edge)	0	20	ns
$t_{v(MO)}$	Data output valid time	Master mode(after enable edge)	-	5	ns

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{h(SO)}$	Data output hold time	Slave mode(after enable edge)	2	-	ns
$t_{h(MO)}$		Master mode(after enable edge)	1	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	45	55	%

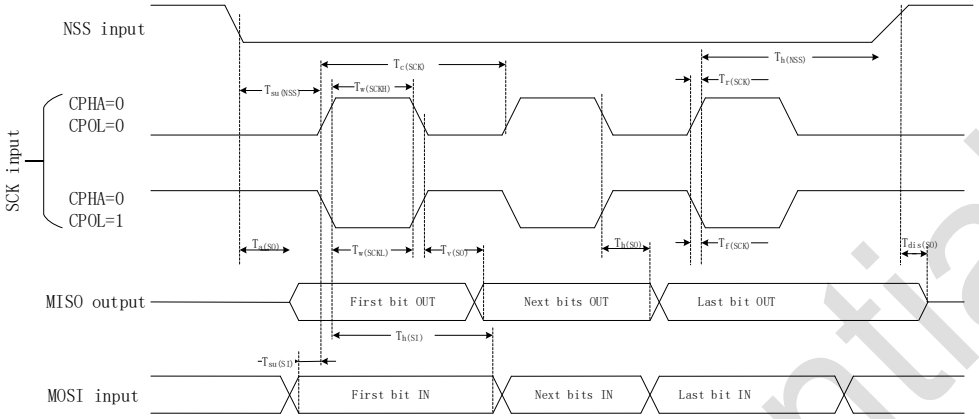


Figure 5-4 SPI timing diagram – Slave mode and CPHA=0

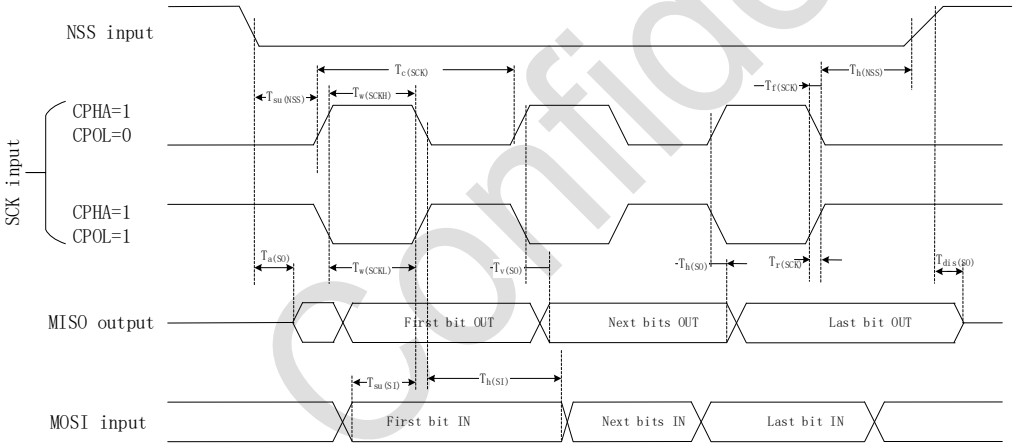


Figure 5-5 SPI timing diagram – Slave mode and CPHA=1

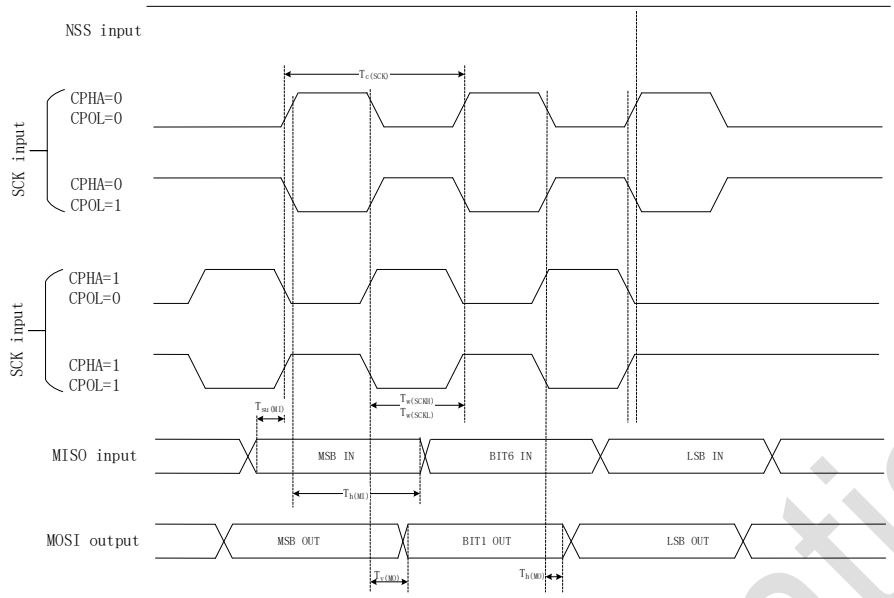


Figure 5-6 SPI timing diagram – Master mode

5.3.23.3. I²S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK}	I²S clock frequency	Master mode(data: 16 bits, audio frequency=48 kHz)	1.597	1.601	MHz
		Slave mode	0	7	
$t_{r(ck)}$	I²S clock rise time	Capacitive load: C_L = 15 pF	-	5	ns
$t_{f(ck)}$	I²S clock fall time	Capacitive load: C_L = 15 pF	-	6	
$t_{w(CKH)}$	I²S clock high time	Master f_{PCLK} = 16 MHz, audio frequency = 48 kHz	306	-	
$t_{w(CKL)}$	I²S clock low time	Master f_{PCLK} = 16 MHz, audio frequency = 48 kHz	312	-	
$t_{v(WS)}$	WS valid time	Master mode	2	-	
$t_{h(WS)}$	WS hold time	Master mode	2	-	
$t_{su(WS)}$	WS setup time	Slave mode	7	-	
$t_{h(WS)}$	WS hold time	Slave mode	1	-	
$t_{su(SD\_MR)}$	Data input setup time	Master mode	11.5	-	
$t_{su(SD\_SR)}$		Slave mode	2	-	
$t_{h(SD\_MR)}$	Data input hold time	Master mode	0	-	
$t_{h(SD\_SR)}$		Slave mode	0	-	
$t_{v(SD\_MT)}$	Data output valid time	Master mode	-	17	
$t_{v(SD\_ST)}$		Slave mode	-	9	
$t_{h(SD\_MT)}$	Data output hold time	Master mode	4	-	
$t_{h(SD\_ST)}$		Slave mode	6	-	
DuCy(sck)	I²S slave input clock duty cycle	Slave mode	45	55	%

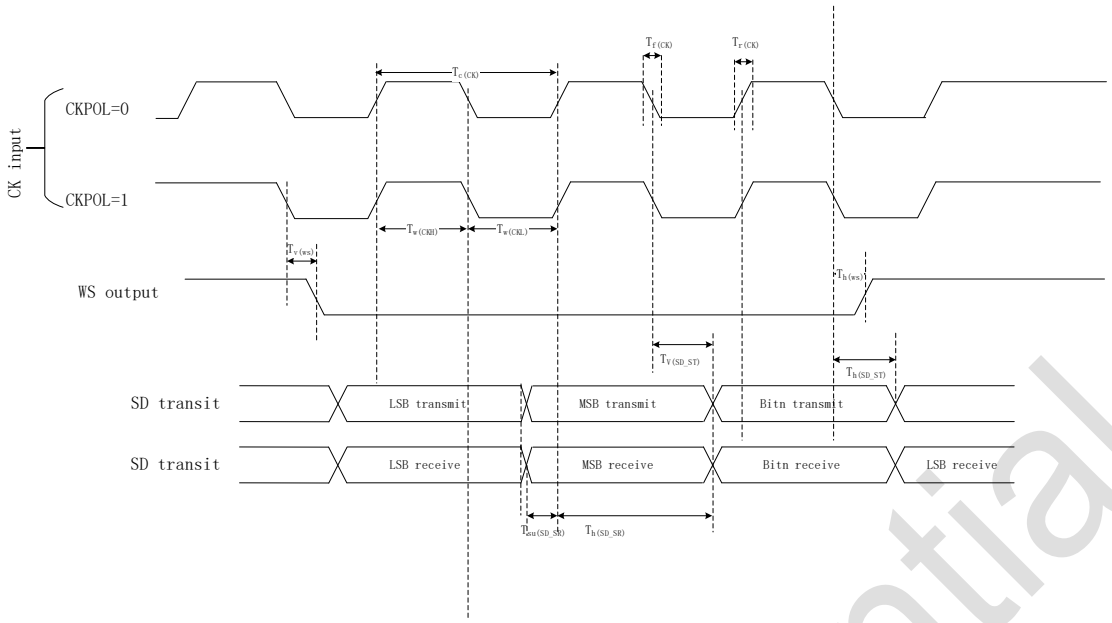


Figure 5-7 I²S timing diagram – Master mode(Philips protocol)

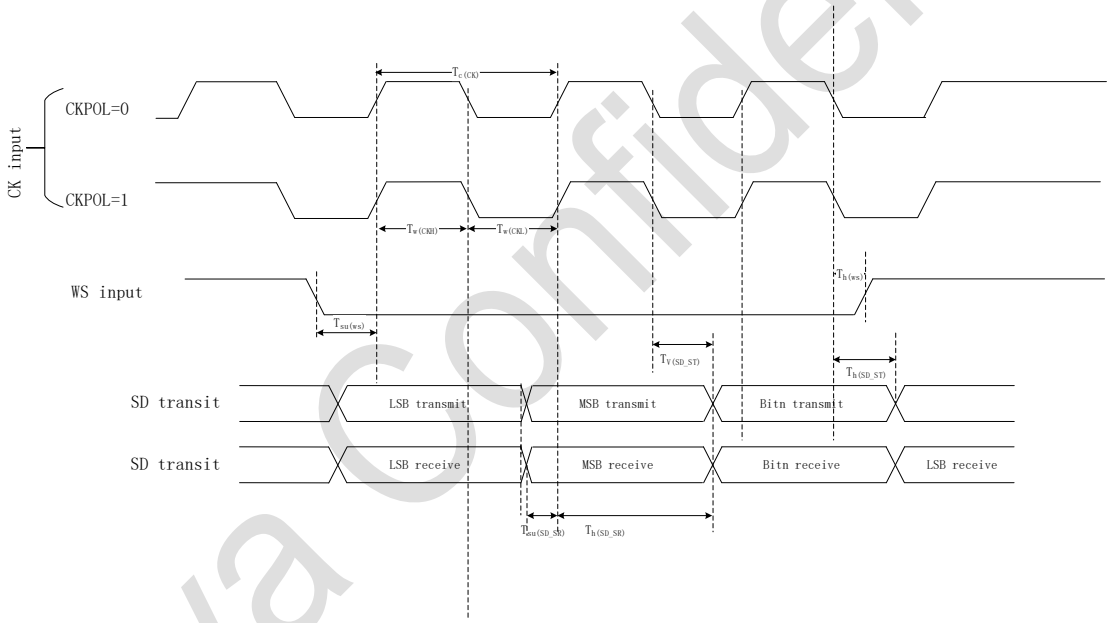


Figure 5-8 I²S timing diagram – Slave mode(Philips protocol)

5.3.23.4. USB characteristics

Table 5-41 USB electrical characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{CCA}	USB transceiver operating voltage	-	3.0	-	3.6	V
R_{PUUSB1}(1)	Pull-up resistance when bus is idle, USB_IDLE=1	-	900	1200	1500	Ω
R_{PUUSB2}(1)	Pull-up resistance when transmitting, USB_IDLE=0	-	1500	2200	3000	Ω

1. RPUUSB1, RPUUSB2 includes ESD resistor to PAD

Table 5-42 USB AC characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit

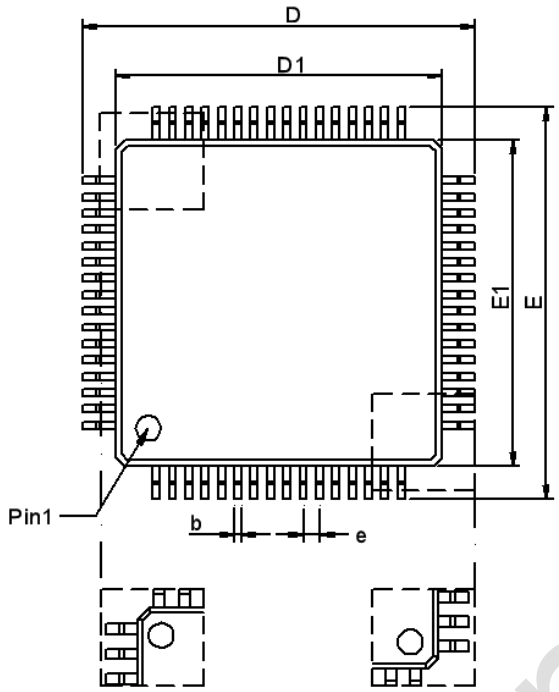
t_{FR}	Rise time	C_L=50 ~ 125 pF 10% to 90% of $\|V_{OH}-V_{OL}\|$	4	-	20	ns
t_{FF}	Fall time	C_L=50 ~ 125 pF 90% to 10% of $\|V_{OH}-V_{OL}\|$	4	-	20	ns
FRFM	Differential rise and fall time matching (t_{FR}/t_{FF})	Excluding the first transition from idle state	90	-	111.1	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle state	1.3	-	2.0	V

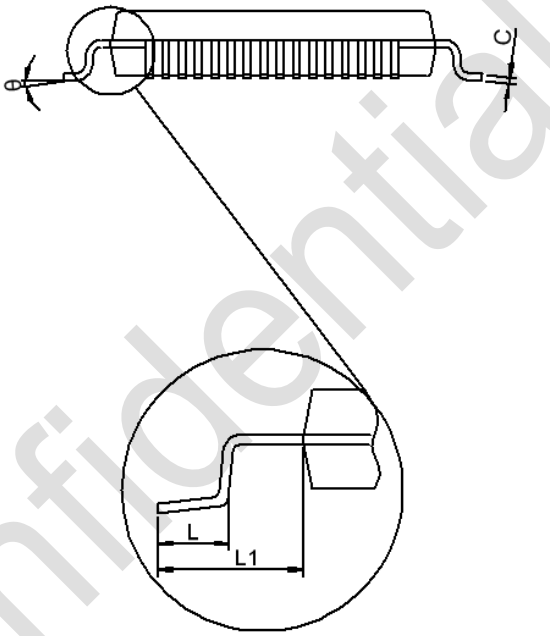
5.3.23.5. CAN 2.0 characteristics

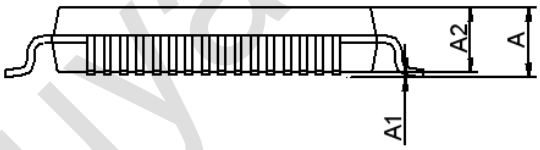
Refer to I/O port characteristics for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6. Package Information

6.1. LQFP64 package size







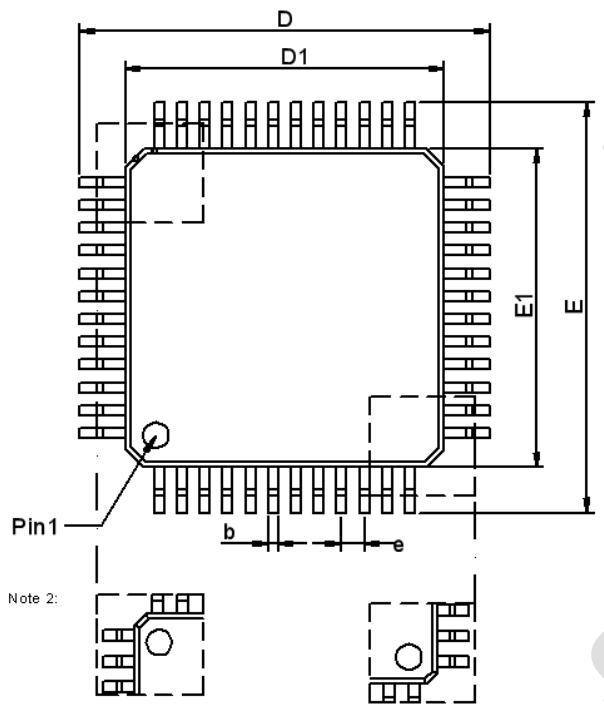
Common Dimensions
(Unit of Measure=millimeters)

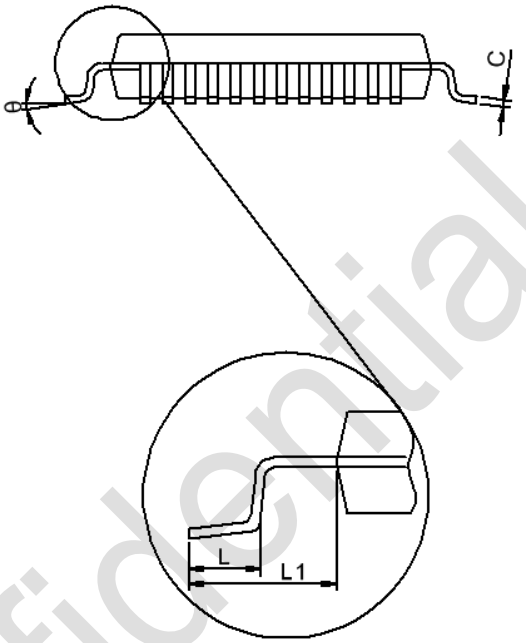
Symbol	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.180	-	0.270
c	0.130	-	0.180
D	11.950	12.000	12.050
D1	9.900	10.000	10.100
E	11.950	12.000	12.050
E1	9.900	10.000	10.100
e		0.500BSC	
L	0.530	-	0.700
L1		1.000REF	
θ	0	-	7°

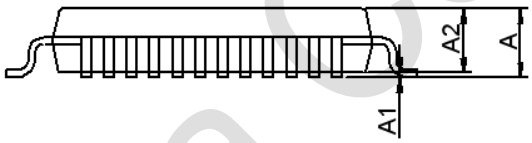
Note：1. Dimensions are not to scale
2.Have two shape can be compatible with each other

	TITLE	DRAWING NO.	REV
PUYA	Puya LQFP64L 10x10X1.4-0.5PITCH	QRPD-0051	1.1

6.2. LQFP48 package size







Common Dimensions

(Unit of Measure=millimeters)

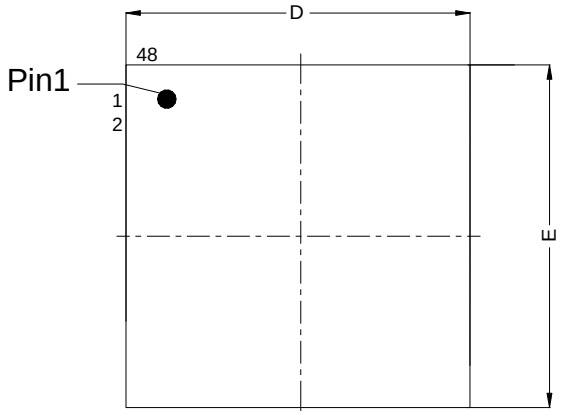
Symbol	Min	Typ	Max
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.180	-	0.270
c	0.130	-	0.180
D	8.800	9.000	9.200
D1	6.900	7.000	7.100
E	8.800	9.000	9.200
E1	6.900	7.000	7.100
e		0.500BSC	
L	0.450	-	0.750
L1		1.000REF	
θ	0	-	7°

Note：1. Dimensions are not to scale
2.Have two shape can be compatible with each other

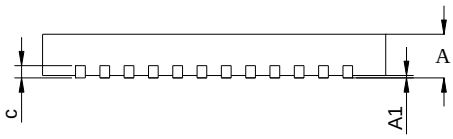
	TITLE	DRAWING NO.	REV
PUYA	Puya LQFP48L 7x7X1.4-0.5PITCH	QRPD-0050	1.1

6.3. QFN48 package size

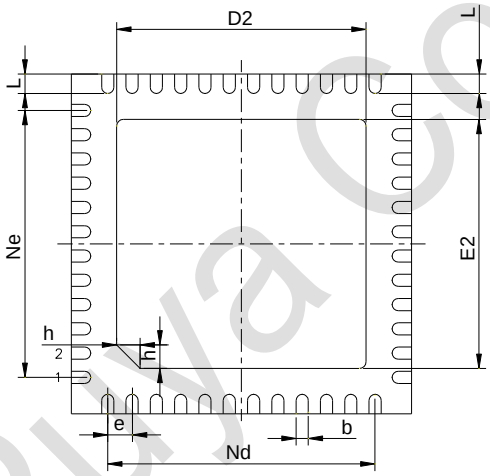
TOP VIEW



SIDE VIEW



BOTTOM VIEW



Common Dimensions
(Unit of Measure=millimeters)

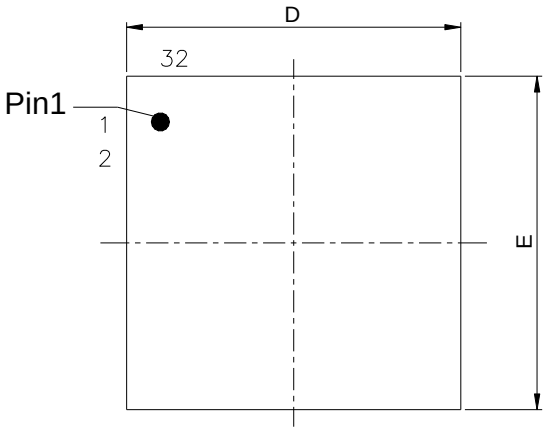
Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
c		0.200REF	
D	5.900	6.000	6.100
D2	4.100	4.300	4.500
E	5.900	6.000	6.100
E2	4.100	4.300	4.500
e		0.400BSC	
Nd		4.400BSC	
Ne		4.400BSC	
L	0.300	0.400	0.500
h	0.300	0.350	0.400

Note：1. Dimensions are not to scale

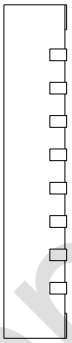
	TITLE	DRAWING NO.	REV
PUYA	Puya QFN48L 6X6X0.75-0.4PITCH POD	QRPD-0056	1.1

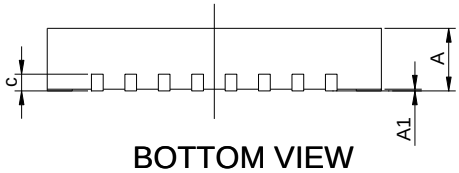
6.4. QFN32(4*4) package size

TOP VIEW

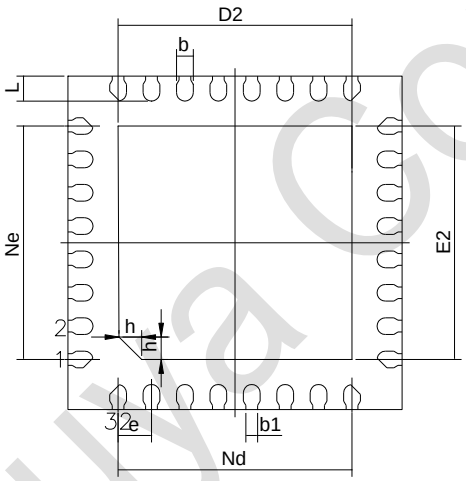


SIDE VIEW





BOTTOM VIEW



Common Dimensions

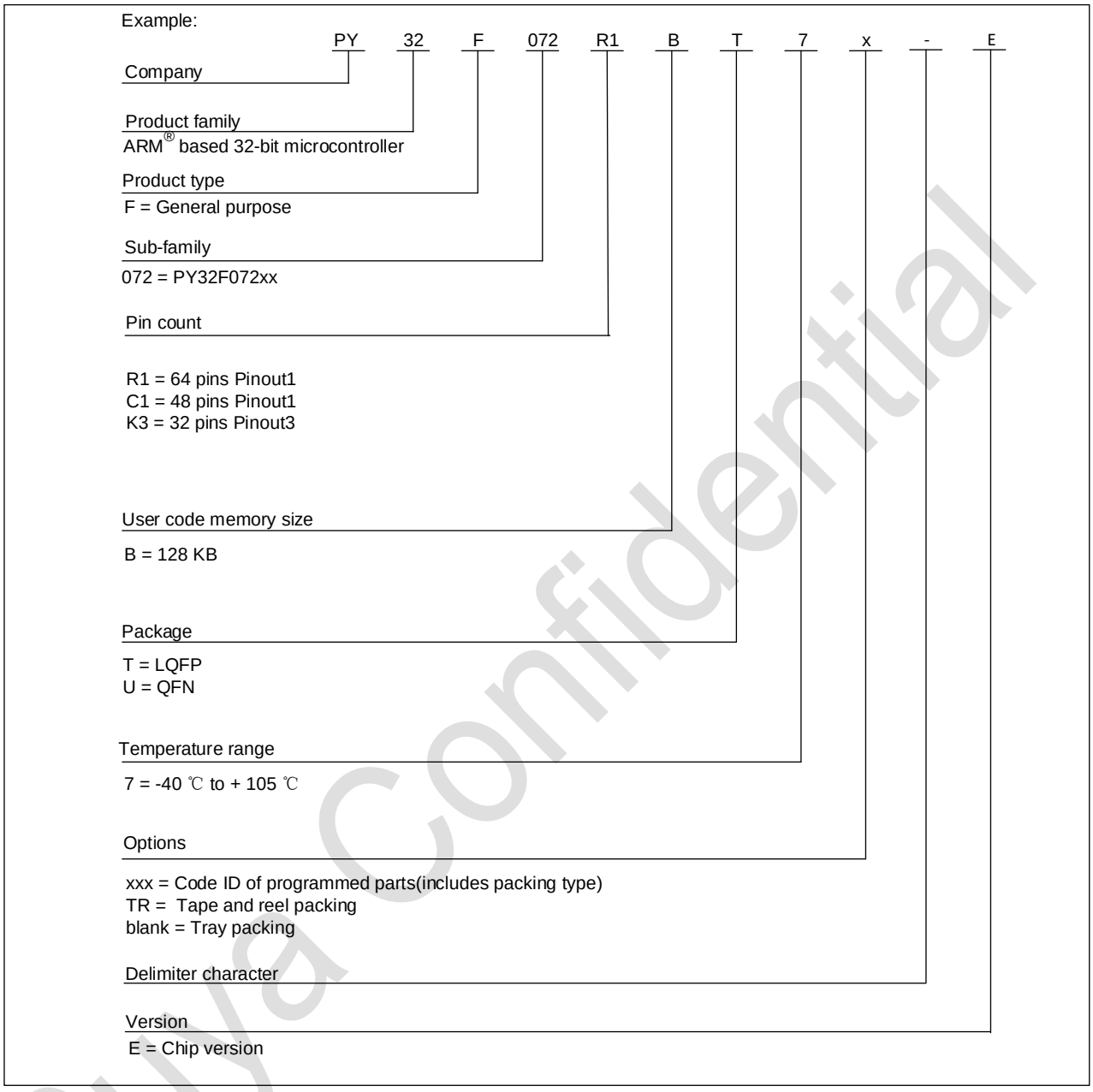
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
c	0.180	0.200	0.250
D	3.900	4.000	4.100
D2	2.700	2.850	3.000
E	3.900	4.000	4.100
E2	2.700	2.850	3.000
e	0.400BSC		
Nd	2.800BSC		
Ne	2.800BSC		
b1	0.140REF		
L	0.200	0.300	0.400
h	0.300	0.350	0.400

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	Puya QFN32L 4X4X0.75-0.4PITCH POD	QRPD-0060	1.0

7. Ordering Information



8. Version History

Version	Date	Updated Record
V1.0	2024.12.25	1. Initial version
V1.1	2025.02.11	1. Update ordering information

Puya Semiconductor Co., Ltd.