P24CM02F

I²C-Compatible Serial E²PROM

Datasheet Rev.1.7

General Description

The P24CM02F is I²C-compatible Serial EEPROM (Electrically Erasable Programmable Memory) device. It contains a memory array of 2048 Kbits (256 Kbytes), which is organized in 256 bytes per page.

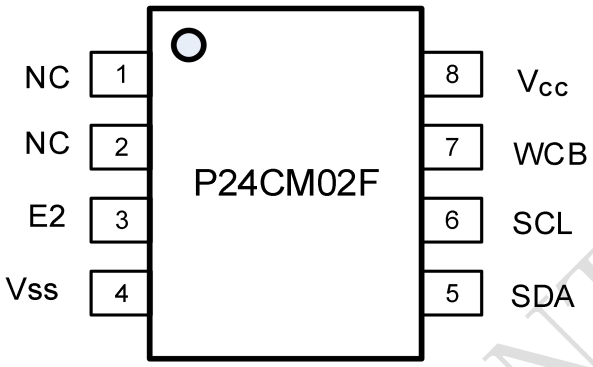
Features

- Single Supply Voltage and High Speed Mode
  - ✧ Minimum operating voltage down to 1.65V
  - ✧ 400kHz/1MHz clock from 1.65 V to 3.6 V
  - ✧ 3.4MHz clock from 1.65 V to 3.6 V
- Low power CMOS technology
  - ✧ Read current 0.8mA (400kHz, typical)
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Transparent ECC on each group of four bytes which can correct 1-bit error
- Sequential & Random Read Features
- Additional write lockable page (Identification page)
- Additional 128 bits Serial Number (Unique ID)
- 256 bytes Page Write Modes, Partial Page Writes Allowed
- Write protect of the whole memory array
- Self-timed Write Cycle (5ms maximum)
- High Reliability
  - ✧ Endurance: 1 Million Write Cycles
  - ✧ Data Retention: 100 Years
  - ✧ HBM: 4 kV
  - ✧ Latch up Capability: +/- 200mA(25C)
- Package: SOP8, TSSOP8, UDFN8, WLCSP8

1. Pin Configuration

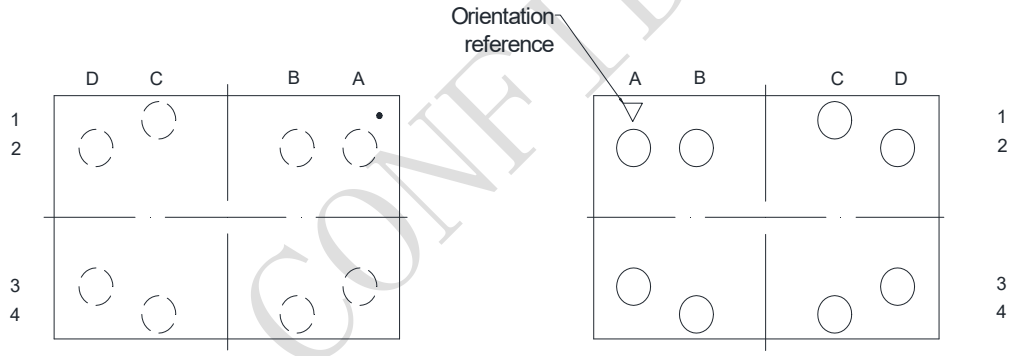
1.1 Pin Configuration

Figure 1-1 Pin Configuration



SOP8/TSSOP8/UDFN8

TOP VIEW **BOTTOM VIEW**



WLCSP8

1.2 Pin Definition

Table 1-1 SOP8/TSSOP8/UDFN8 Pin Definition

Pin	Name	Type	Description
1	NC	/	No Connect
2	NC	/	No Connect
3	E2	Input	Slave Address Setting
4	Vss	Ground	Ground
5	SDA	I/O	Serial Data Input and Serial Data Output
6	SCL	Input	Serial Clock Input
7	WCB	Input	Write Control, Low Enable Write
8	Vcc	Power	Power

Table 1-2 WLCSP8 Pin Definition

Pin	Name	Type	Description
A3	NC	/	No Connect
B4	NC	/	No Connect
C4	E2	Input	Slave Address Setting
D3	Vss	Ground	Ground
D2	SDA	I/O	Serial Data Input and Serial Data Output
C1	SCL	Input	Serial Clock Input
B2	WCB	Input	Write Control, Low Enable Write
A2	V_{CC}	Power	Power Supply

1.3 Pin Descriptions

Serial Clock (SCL): The SCL input is used to positive-edge clock data in and negative-edge clock data out.

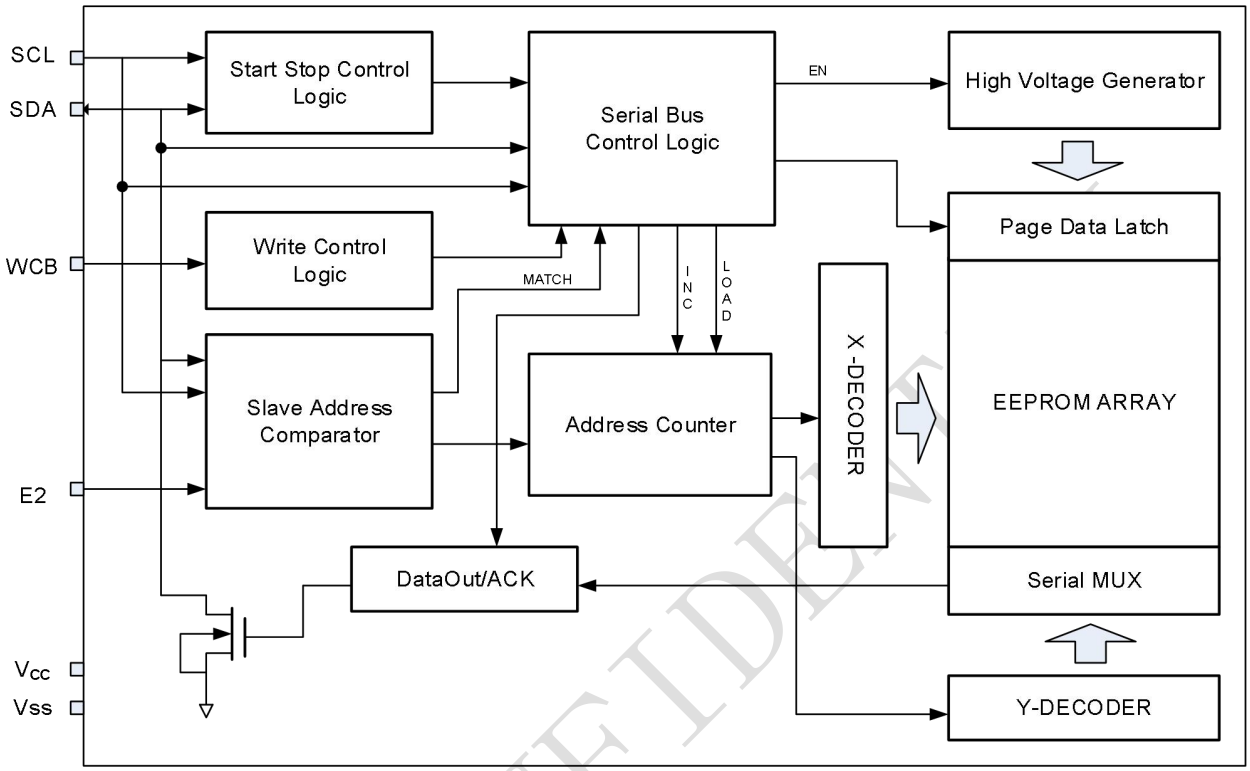
Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-OR'ed with any number of other open-drain or open-collector devices.

Device Addresses (E2): The E2 pin is device address inputs. Typically, the E2 pin is for hardware addressing and a total of 2 devices can be connected on a single bus system. If the pin is left floating, the E2 pin will be internally pulled down to Vss.

Write Control (WCB): The Write Control input, when WCB is connected directly to V_{CC}, all write operations to the memory are inhibited. When connected to Vss, allows normal write operations. If the pin is left floating, the WCB pin will be internally pulled down to Vss.

2. Block Diagram

Figure 2-1 Block Diagram



3. Electrical Characteristics

Table 3-1 Absolute Maximum Ratings [1]

Symbol	Parameter	Min.	Max.	Units
T_{STG}	Storage Temperature	-65	150	°C
T_A	Ambient operating temperature	-40	105	°C
V_{CC}	Supply Voltage	-0.5	4.0	V
V_{IO}	Input or output range	-0.5	4.0	V
I_{OL}	DC output current (SDA=0)	-	5	mA

Note: [1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3-2 Pin Capacitance [1]

Symbol	Parameter	Max.	Units	Test Condition
$C_{I/O}$	Input/output Capacitance (SDA)	8	pF	$V_{I/O}$ = Vss
C_{IN}	Input Capacitance (SCL)	6	pF	V_{IN} = Vss

Note: [1] Test Conditions: T_A= 25°C, f_{SCL} = 1MHz, Vcc =3.6V.

Table 3-3 DC Characteristics (Unless otherwise specified, V_{CC} = 1.65 V to 3.6V, T_A= -40°C to+105°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{CC}	Supply Voltage	1.65	-	3.6	V	
Isb	Standby Current (Standby mode)	-	0.8	3.0	uA	V_{CC} = 1.8V, Vin = V_{SS} or V_{CC} Device is not selected
		-	1.2	5.0	uA	V_{CC} = 2.5V, Vin = V_{SS} or V_{CC} Device is not selected
		-	-	12.0	uA	V_{CC} = 3.6V, Vin = V_{SS} or V_{CC} Device is not selected
		-	-	20.0	uA	V_{CC} = 3.6V, Vin = V_{SS} or V_{CC}, T_A=105°C Device is not selected
I_{CC1}	Supply Current(Read)	-	0.8	2.0	mA	V_{CC} = 1.8 V, f_{SCL} = 400 KHz
		-	0.9	2.5	mA	V_{CC} = 2.5 V, f_{SCL} = 400 KHz
		-	1	3.0	mA	V_{CC} = 3.6 V, f_{SCL} = 1 MHz
		-	1.6	8.0	mA	V_{CC} = 3.6 V, f_{SCL} = 3.4 MHz
I_{CC2}	Supply Current(Write)	-	1.5	4.0	mA	Average value during t_W, 1.65V < V_{CC}< 3.6 V
I_{LI}	Input Leakage Current	-2	-	+2.0	μA	V_{IN} = V_{CC} or Vss, device in standby mode
I_{LO}	Output Leakage Current	-2	-	+2.0	μA	SDA in Hi-Z, external voltage applied on SDA: VSS or VCC
V_{IL}	Input Low Voltage	-0.45	-	0.3 V_{CC}	V	SCL, SDA
V_{IH}	Input High Voltage	0.7V_{CC}	-	V_{CC}+0.5	V	SCL, SDA
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL} = 2.1 mA, V_{CC} = 2.5 V

Table 3-4 Fast Mode AC Characteristics (T_A = -40 °C to +105 °C)

Symbol	Parameter	1.65≤V_{CC}≤3.6			1.65≤V_{CC}≤3.6			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Clock Frequency	-	-	400	-	-	1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3	-	-	0.55	-	-	μs
t_{HIGH}	Clock Pulse Width High	0.6	-	-	0.3	-	-	μs
t_{AA}	Clock Low to Data Out Valid	0.05	-	0.9	0.05	-	0.50	μs
t_I	Noise Suppression Time	-	-	0.05	-	-	0.05	μs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3	-	-	0.5	-	-	μs
$t_{HD.STA}$	Start Hold Time	0.6	-	-	0.25	-	-	μs
$t_{SU.STA}$	Start Setup Time	0.6	-	-	0.25	-	-	μs
$t_{HD.DAT}$	Data in Hold Time	0	-	-	0	-	-	μs
$t_{SU.DAT}$	Data in Setup Time	0.1	-	-	0.08	-	-	μs
t_R	Inputs Rise Time[1]	-	-	0.3	-	-	0.3	μs
t_F	Inputs Fall Time[1]	-	-	0.3	-	-	0.3	μs
$t_{SU.STO}$	Stop Setup Time	0.6	-	-	0.25	-	-	μs
t_{DH}	Data Out Hold Time	0.05	-	-	0.05	-	-	μs
$t_{SU.WCB}$	WCB pin Setup Time	1	-	-	0.6	-	-	μs
$t_{HD.WCB}$	WCB pin Hold Time	1	-	-	0.6	-	-	μs
t_{WR}	Write Cycle Time	-	-	5	-	-	5	ms

Notes: [1] This parameter is ensured by characterization not 100% tested

[2] AC measurement conditions:

- t_{AA} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 VCC or 0.7 VCC, assuming that Rbus × Cbus time constant is within 400 ns for 0.4 MHz frequency, within 120 ns for 1 MHz frequency
- RL (connect to VCC): 1.3 kΩ
- CL = 100 pF
- Input pulse voltage: 0.2 VCC to 0.8 VCC
- Input rise and fall time: < 50 ns
- Input and output timing reference voltage: 0.3 VCC and 0.7 VCC

Table 3-5 High Speed Mode AC Characteristics (T_A= -40 °C to +105 °C)

Symbol	Parameter	1.65≤V_{CC}≤3.6			Units
		Min.	Typ.	Max.	
f_{SCL}	Clock Frequency	-	-	3400	kHz
t_{LOW}	Clock Pulse Width Low	0.16	-	-	μs
t_{HIGH}	Clock Pulse Width High	0.06	-	-	μs
t_{AA}	Clock Low to Data Out Valid	0.01	-	0.14	μs
t_I	Noise Suppression Time	-	-	0.01	μs
t_{BUF}	Time the bus must be free before a new transmission can start	0.3	-	-	μs
$t_{HD.STA}$	Start Hold Time	0.16	-	-	μs
$t_{SU.STA}$	Start Setup Time	0.16	-	-	μs
$t_{HD.DAT}$	Data in Hold Time	0	-	-	μs
$t_{SU.DAT}$	Data in Setup Time	0.01	-	-	μs
t_R	Inputs Rise Time[1]	0.01	-	0.08	μs
t_F	Inputs Fall Time[1]	0.01	-	0.08	μs
$t_{SU.STO}$	Stop Setup Time	0.16	-	-	μs
t_{DH}	Data Out Hold Time	0.05	-	-	μs
$t_{SU.WCB}$	WCB pin Setup Time	0.6	-	-	μs
$t_{HD.WCB}$	WCB pin Hold Time	0.6	-	-	μs
t_{WR}	Write Cycle Time	-	-	5	ms

Notes: [3] AC measurement conditions:

- t_{AA} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 VCC or 0.7 VCC, assuming that Rbus × Cbus time constant is within 20 ns
- RL (connect to VCC): 1.3 kΩ
- CL = 15 pF
- Input pulse voltage: 0.2 VCC to 0.8 VCC
- Input rise and fall time: < 50 ns
- Input and output timing reference voltage: 0.3 VCC and 0.7 VCC

Table 3-6 Reliability Characteristic [1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
EDR[2]	Endurance	1,000,000			Write cycles
DRET[3]	Data retention	100			Years

Note: [1] This parameter is ensured by characterization and is not 100% tested

[2] Under the condition: 3.3V, Page mode

[3] Test condition: T_A = 25°C

Figure 3-1 Bus Timing

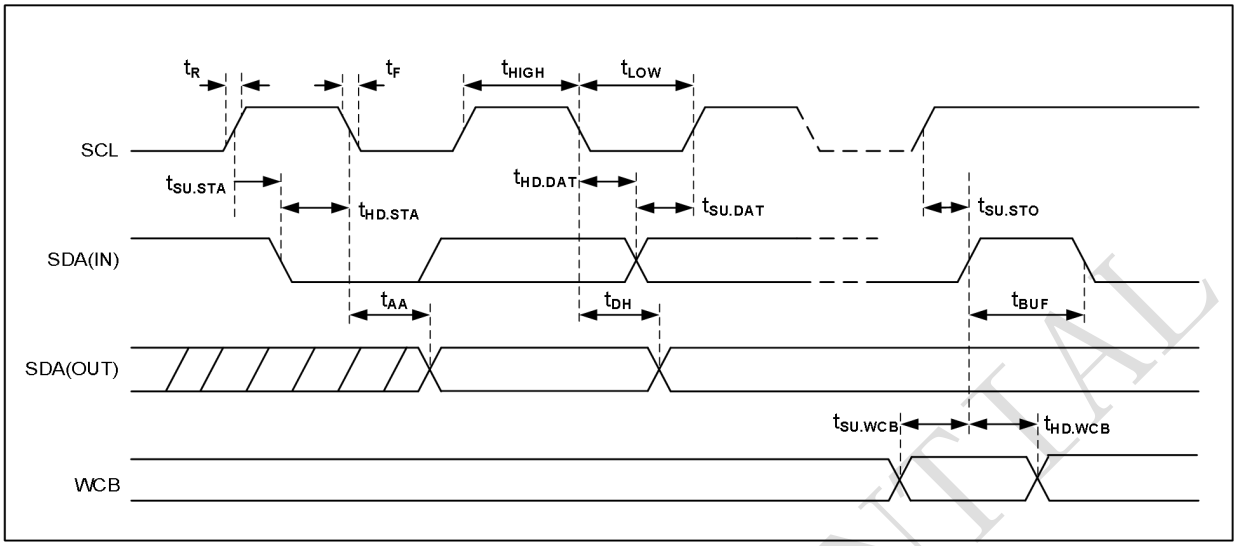
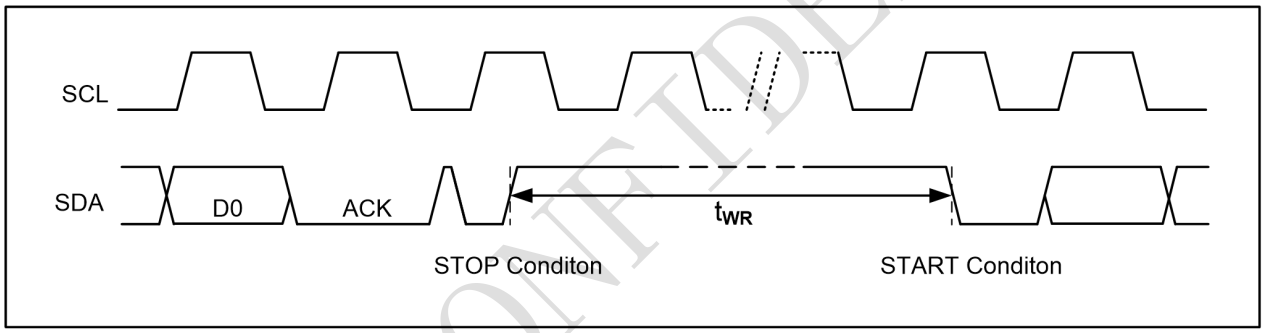


Figure 3-2 Write Cycle Timing



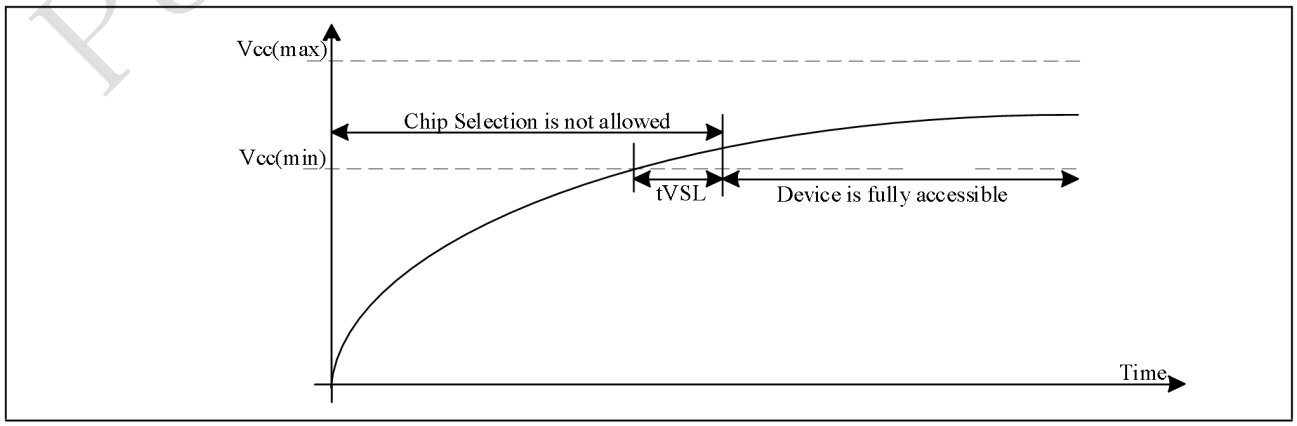
Note: [1] The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal write cycle.

Device Power-Up

The EEPROM has a built-in power-on-reset circuit that initializes itself at the same time during power-on. Unsuccessful initialization may cause a malfunction. To operate the power-on-reset circuit normally, the following conditions must be satisfied to raise the power supply voltage.

When initialization is successfully completed by the power-on-reset circuit, the EEPROM enters the standby status. tVSL is the time required to initialize the EEPROM. No instructions are accepted during this time.

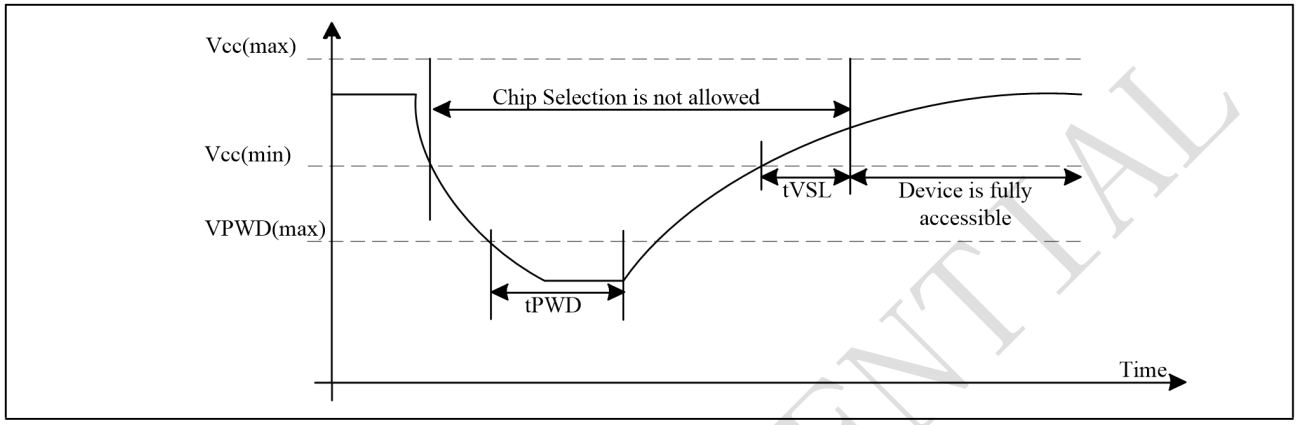
Figure 3-3 Power up Timing



Power Up/Down and Voltage Drop

For Power-down to Power-up operation, the VCC of EEPROM device must below VPWD for at least tPWD timing. Please check the table below for more detail.

Figure 3-4 Power down-up Timing



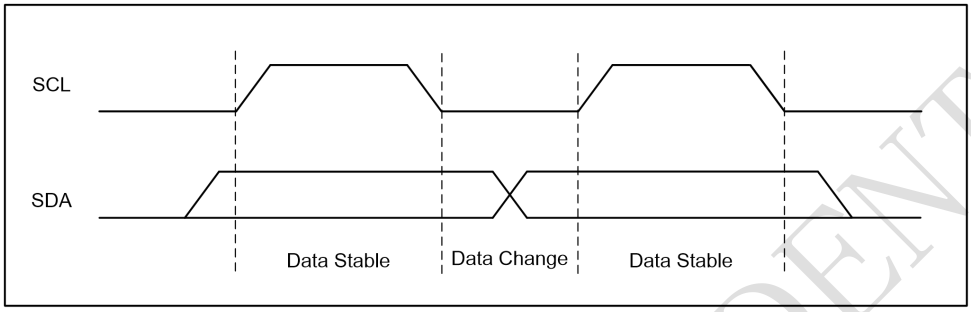
Symbol	Parameter	min	max	unit
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		0.7	V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVSL	VCC(min.) to device operation	100		us
tVR	VCC Rise Time	1	500000	us/V

4. Device Operation

4.1 Data Input

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 4-1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

Figure 4-1 Data Validity



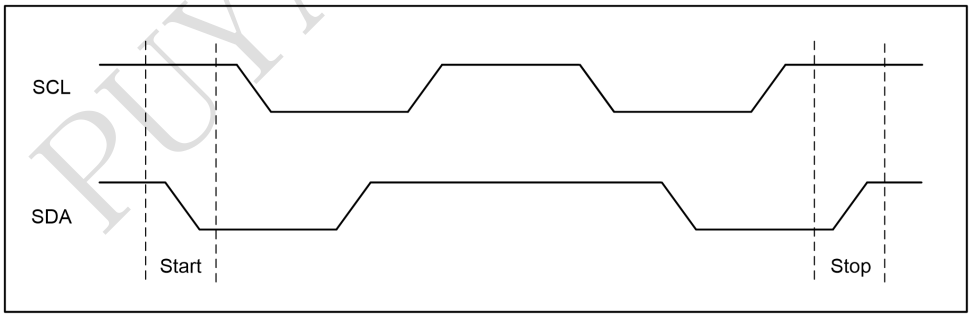
4.2 Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 4-2).

4.3 Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the P24CM02F in a standby mode (see Figure 4-2).

Figure 4-2 Start and Stop Definition

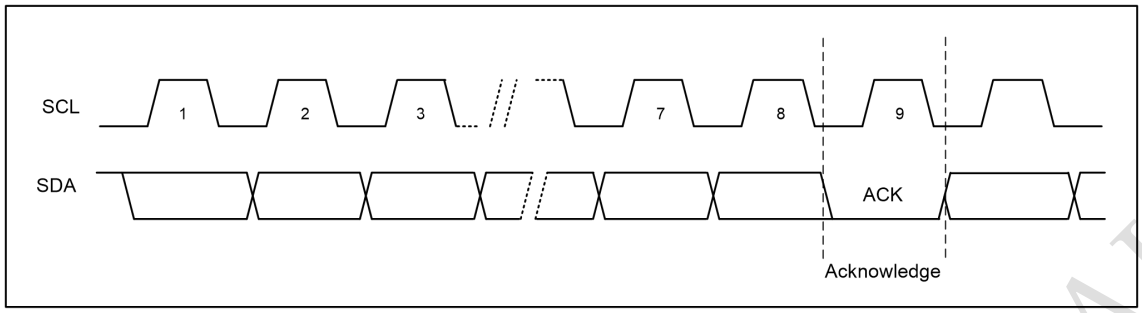


4.4 Acknowledge (ACK)

All addresses and data words are serially transmitted to and from the P24CM02F in 8-bit words. The P24CM02F sends a “0” to acknowledge that it has received each word. This happens during the ninth clock

cycle.

Figure 4-3 Output Acknowledge



4.5 Power Up Sequence

During a power-up sequence, the VCC supplied to P24CM02F should monotonically rise from Vss to the minimum VCC level with a slew rate no greater than 1us/V.

To prevent inadvertent write operations or other spurious events from happening during a power-up sequence, the P24CM02F includes a power-on-reset circuit. Upon power-up, the device will not respond to any commands until the VCC level crosses the internal voltage threshold and waiting 100μs that brings the device out of reset and into standby mode.

4.6 Standby Mode

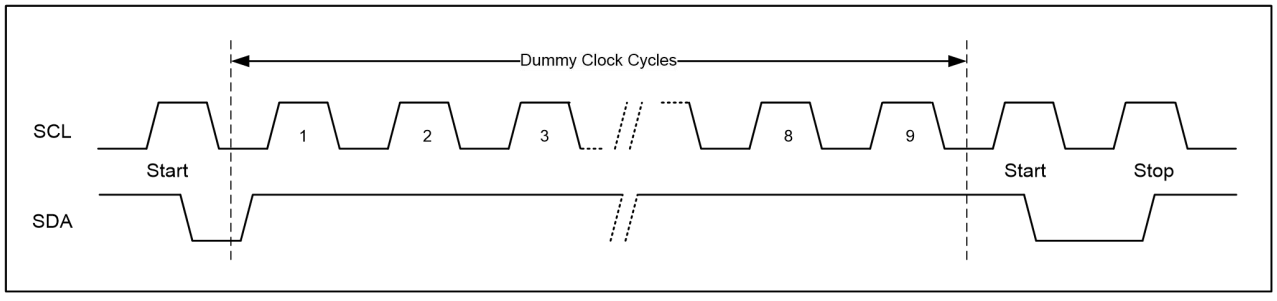
The P24CM02F features a low-power standby mode which is enabled:

(a) after a fresh power up, (b) after receiving a STOP bit in read mode, and (c) after completing a self-time internal programming operation.

4.7 Soft Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps: (a) Create a start condition, (b) Clock nine cycles, and (c) create another start bit followed by stop bit condition, as shown below. The device is ready for the next communication after the above steps have been completed.

Figure 4-4 Soft Reset



4.8 Device Addressing

The P24CM02F requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Table 4-1/4-2/4-3). The device address word consists of a mandatory one-zero sequence for the first four most-significant bits, as shown.

Table 4-1 Device Address

Chip	Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P24CM02F	Normal Area	1	0	1	0	E2	A17	A16	R/W
	ID Page	1	0	1	1	E2	X	X	R/W
	Lock Bit	1	0	1	1	E2	X	X	R/W
	Serial Number	1	0	1	1	E2	X	X	1

Table 4-2 Word Address0

Chip	Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P24CM02F	Normal Area	A15	A14	A13	A12	A11	A10	A9	A8
	ID Page	X	X	X	X	0	0	X	X
	Lock Bit	X	X	X	X	X	1	X	X
	Serial Number	X	X	X	X	1	0	X	X

Table 4-3 Word Address1

Chip	Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P24CM02F	Normal Area	A7	A6	A5	A4	A3	A2	A1	A0
	ID Page	A7	A6	A5	A4	A3	A2	A1	A0
	Lock Bit	X	X	X	X	X	X	X	X
	Serial Number	X	X	X	X	A3	A2	A1	A0

The E2 device address bits allow as many as two devices on the same bus. These bits must compare to their corresponding hardwired input pins.

The E2 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are floating.

The seventh (A17) and sixth bit (A16) of the device address is a memory page address bit. This memory page address bit is the most significant bit of the data word address that follows.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, the Chip will output a zero. If a compare is not made, the device will return to a standby state.

4.9 Data Security

P24CM02F has a hardware data protection scheme that allows the user to write protect the whole memory when the WCB pin is at Vcc.

4.10 ECC (Error Correction Code) and Write cycling

The Error Correction Code (ECC) is an internal logic function which is transparent for the I²C-compatible bus communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes [1]. Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

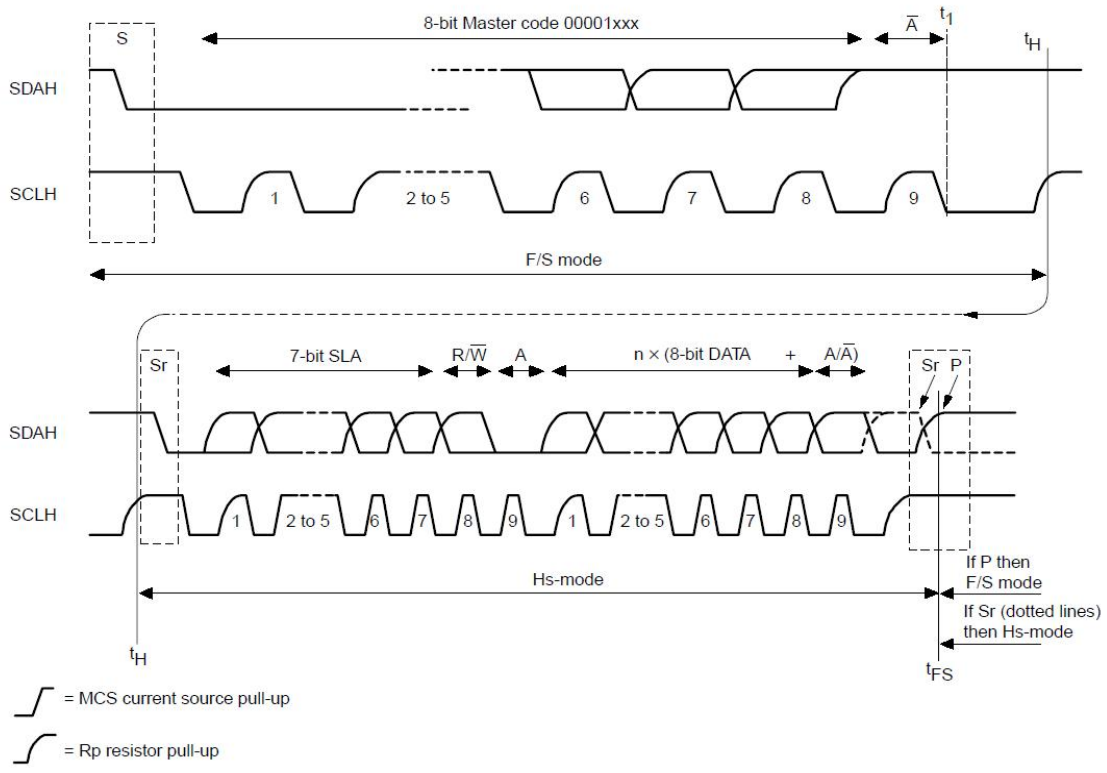
Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group [1]. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the 4 bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value.

Note: [1] A group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer

4.11 High Speed Mode (HS-mode)

TheP24CM02F supports 3.4 MHz high speed mode. A master code (00001XXXb) must be issued to place the device into high speed mode. Communication between master and slave will then be enabled for speeds up to 3.4 MHz. A STOP condition will exit HS-mode. Single- and multiple-byte reads and writes are supported.

Figure 4-6 High Speed Mode Communication



Sr: Repeated Start Flag

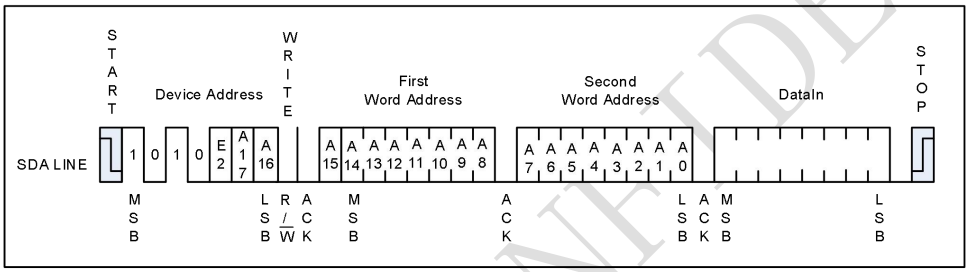
5. Instructions

5.1 Write Operations

5.1.1 Byte Write

A write operation requires 18-bit data word address following the device address word and acknowledgment. The word address field consists of the A17~A16 bit in the device address byte, then the most significant word address (A15~A8) followed by the least significant word address (A7~A0). Upon receipt of this address, the P24CM02F will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the P24CM02F will output a “0” and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. And then the P24CM02F enters an internally timed write cycle, all inputs are disabled during this write cycle and the P24CM02F will not respond until the write is complete (see Figure 5-1).

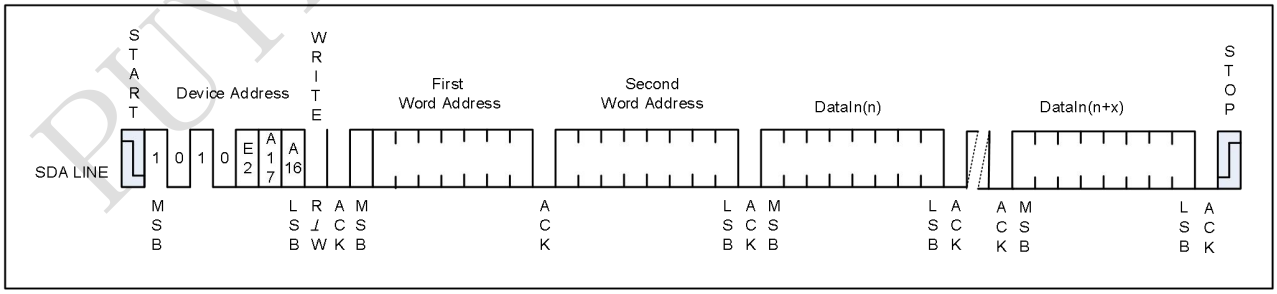
Figure 5-1 Byte Write



5.1.2 Page Write

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the P24CM02F acknowledges receipt of the first data word, the master can transmit more data words. The P24CM02F will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition.

Figure 5-2 Page Write



The lower eight bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 256 data words are transmitted to the P24CM02F, the data word address will roll-over, and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

5.1.3 Acknowledge Polling

Once the internally timed write cycle has started and the P24CM02F inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the P24CM02F respond with a “0”, allowing the read or write sequence to continue.

5.1.4 Write Identification Page

The Identification Page (256 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- MSB address bits A16~A8 are don’t care except for address bit A11 and A10 which must be ‘0’.

LSB address bits A7~A0 define the byte address inside the Identification page. If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoACK).

5.1.5 Lock Identification Page

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Device type identifier = 1011b
- Address bit A10 must be ‘1’; all other address bits are don’t care
- The data byte must be equal to the binary value xxxx xx1x, where x is don’t care

5.2 Read Operations

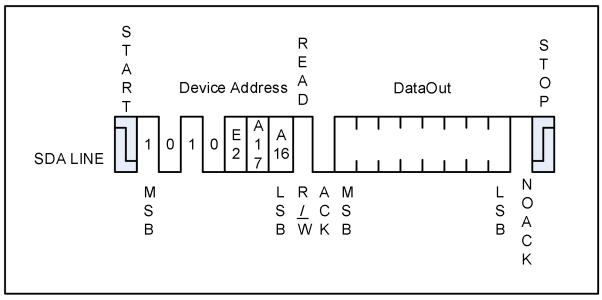
Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to “1”. There are three read operations: Current Address Read; Random Address Read and Sequential Read.

5.2.1 Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to “1” is clocked in and acknowledged by the P24CM02F, the current address data word is serially clocked out. The microcontroller does not respond with an input “0” but does generate a following stop condition (see Figure 5-3).

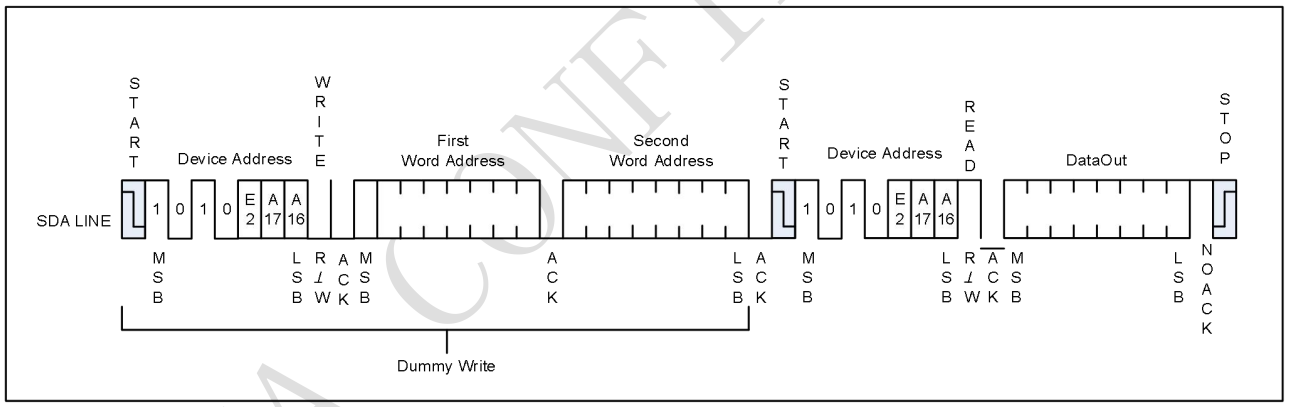
Figure 5-3 Current Address Read



5.2.2 Random Read

A Random Read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the P24CM02F, the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The P24CM02F acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 5-4).

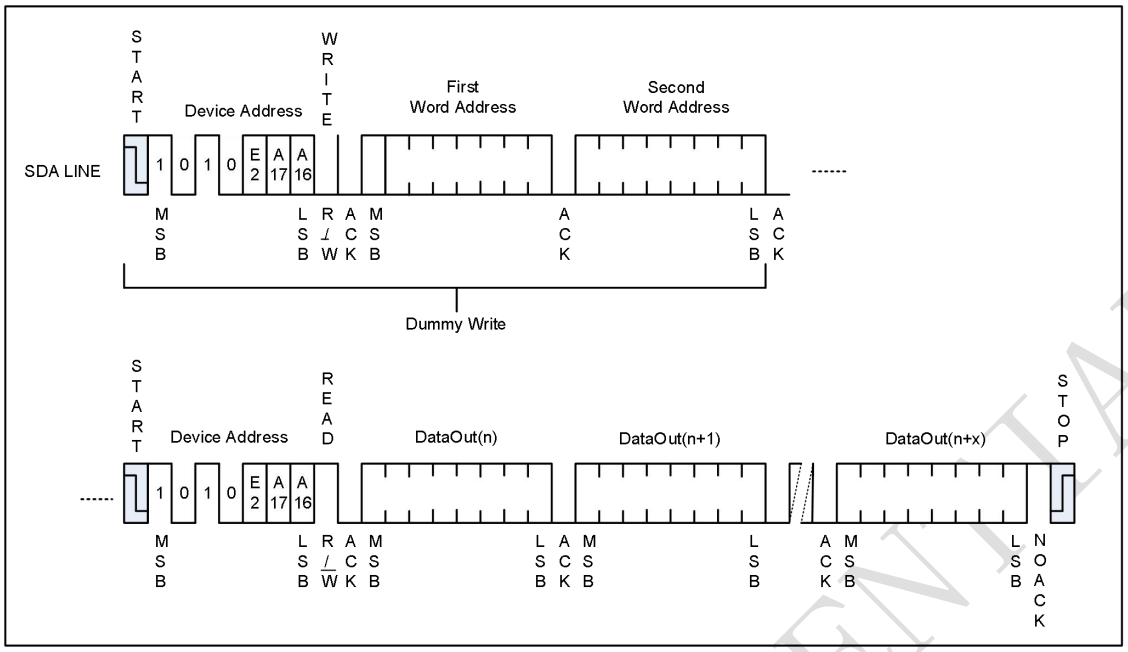
Figure 5-4 Random Read



5.2.3 Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the P24CM02F receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 5-5).

Figure 5-5 Sequential Read



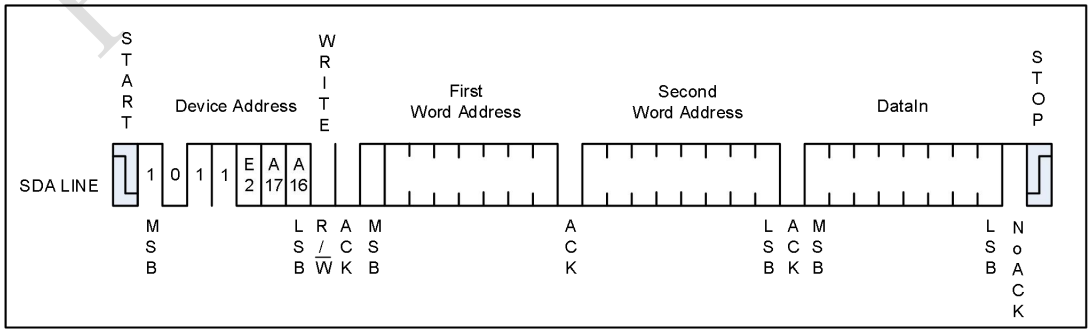
5.2.4 Read Identification Page

The Identification Page (256 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. The Identification Page can be read by Read Identification Page instruction which uses the same protocol and format as the Read Command (from memory array) with device type identifier defined as 1011b. The MSB address bits A16~A8 are don't care, the LSB address bits A7~A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g. when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 246, as the ID page boundary is 256 bytes).

5.2.5 Read Lock Status

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NO-ACK bit if the Identification page is locked.

Figure 5-6 Lock Status Read (When Identification page locked, return NO-ACK after one data byte)



5.2.6 Read Serial Number

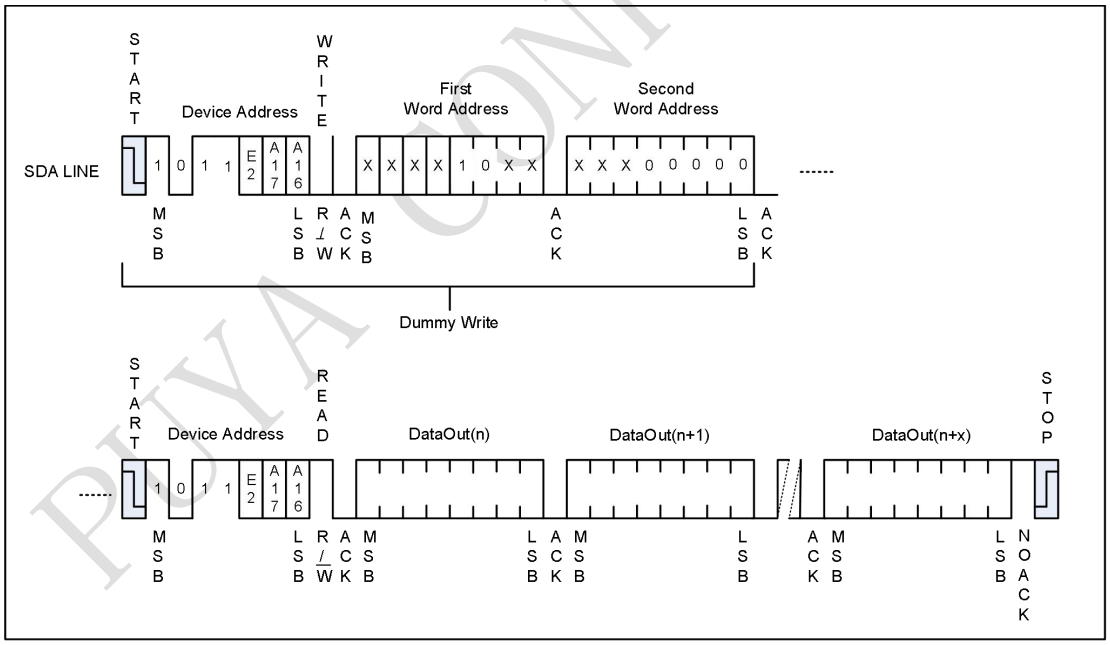
Reading the serial number is similar to the sequential read sequence but requires use of the device address seen in Table 4-1, a dummy write, and the use of a specific word address. The entire 128-bit value must be read from the starting address of the serial number block to guarantee a unique number.

Since the address pointer of the device is shared between the regular EEPROM array and the serial number block, a dummy write sequence, as part of a Random Read or Sequential Read protocol, should be performed to ensure the address pointer is set to zero. A Current Address Read of the serial number block is supported but if the previous operation was to the EEPROM array, the address pointer will retain the last location accessed, incremented by one. Reading the serial number from a location other than the first address of the block will not result in a unique serial number.

Additionally, the word address contains a '10' sequence in bit A11 and A10 of the word address, regardless of the intended address as depicted in Table 4-2. If a word address other than '10' is used, then the device will output undefined data.
Example: If the application desires to read the first byte of the serial number, the word address input would need to be 0800h.

The Serial Number Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (see Figure 5-6)

Figure 5-6 Serial Number Read



Notes: [1] x means don't care bits.

6. Ordering Code Detail

Example: P 2 4 C M02 F – SS H –M I R

Company Designator

P = Puya Semiconductor

Product Series Name

24C = I^2C-compatible Interface EEPROM

Device Density

M02 =2M bits

Device Reversion

F = Version F

Package Option

SS: SOP8

TS: TSSOP8

UN: UDFN8

CS: WLCSP8

Plating Technology

H: RoHS Compliant, Halogen-free

Operation Voltage

M: 1.65~3.6V

N: 1.8~3.6V

Device Grade

I: -40~85C

K: -40~105C

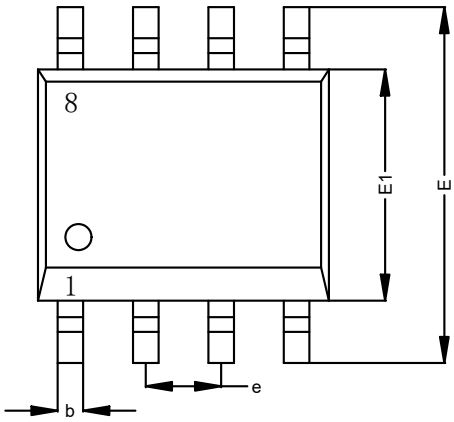
Shipping Carrier Option

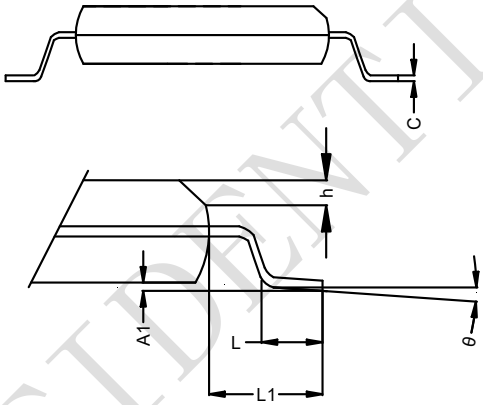
T: TUBE

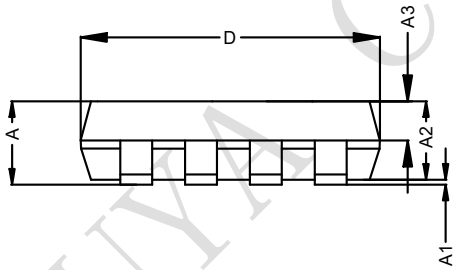
R: TAPE& REEL

7. Package information

7.1 SOP8







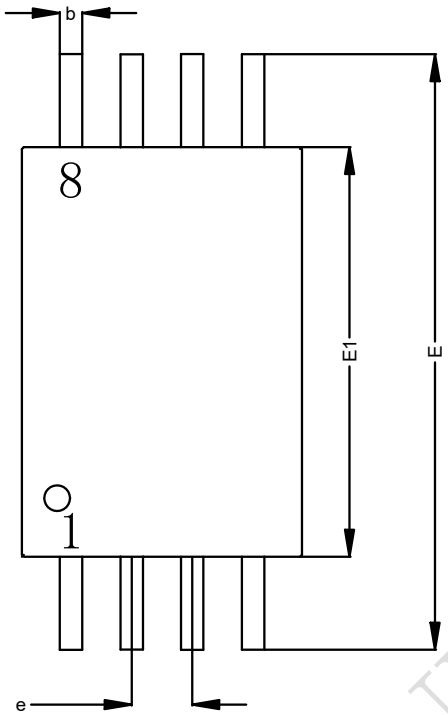
Common Dimensions
(Unit of Measure=millimeters)

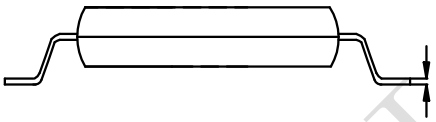
Symbol	Min	Typ	Max
A	-	-	1.750
A1	0.100	-	0.250
A2	1.250	-	-
b	0.310	-	0.510
c	0.170	-	0.250
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
e	-	1.270	-
L	0.400	-	1.270
L1	-	1.050	-
θ	0	-	8°
h	0.25	-	0.50

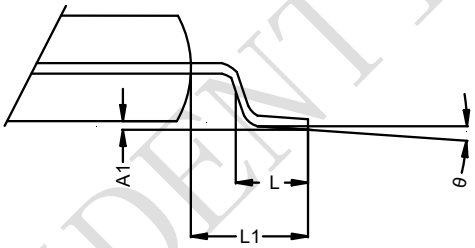
Note：1. Dimensions are not to scale

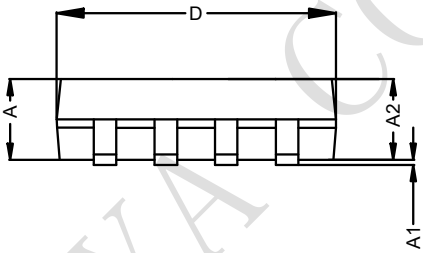
	TITLE	DRAWING NO.	REV
PUYA	Puya SOP8（150mil）POD	QRPD-0004	1.0

7.2 TSSOP8









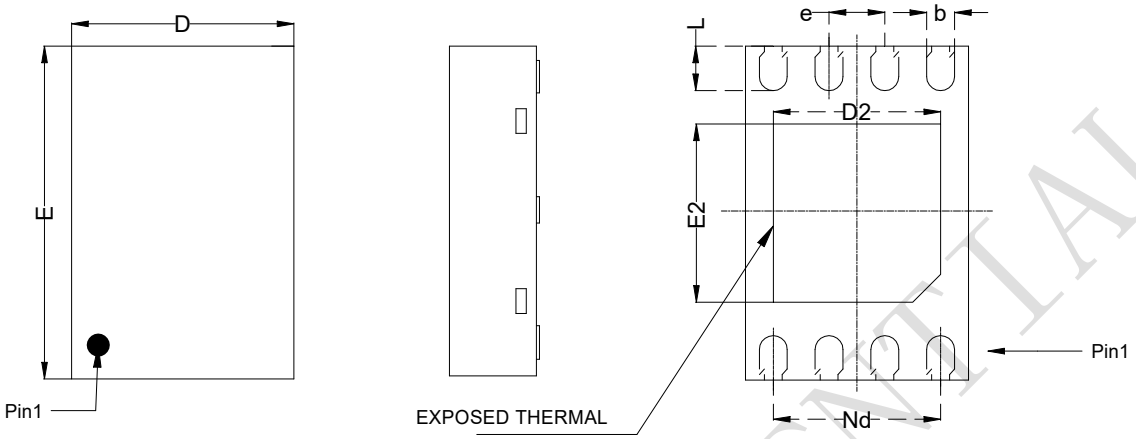
Common Dimensions
(Unit of Measure=millimeters)

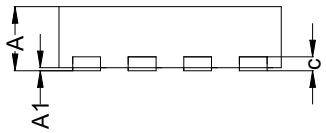
Symbol	Min	Typ	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	1.000	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	2.900	3.000	3.100
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
e	-	0.650	-
L	0.450	-	0.750
L1	-	1.000	-
θ	0	-	8°

Note：1. Dimensions are not to scale

	TITLE	DRAWING NO.	REV
PUYA	PUYA TSSOP8 POD	QRPD-0019	1.0

7.3 UDFN8





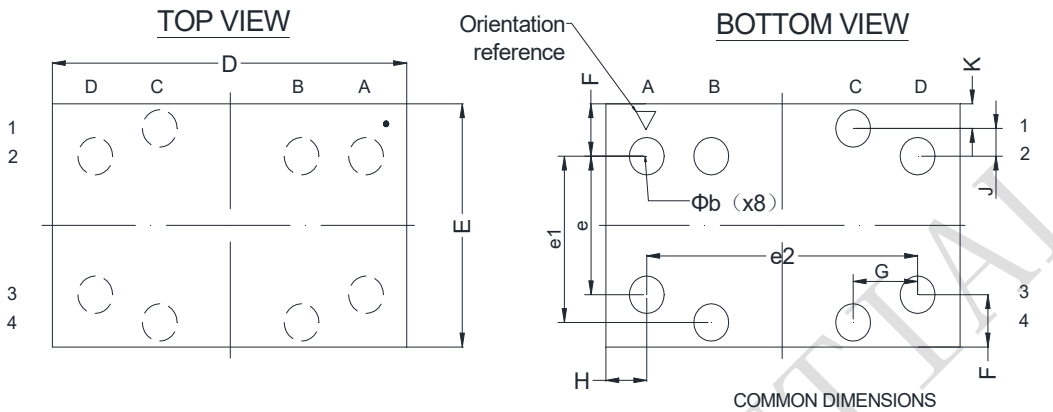
Common Dimensions
(Unit of Measure=millimeters)

Symbol	Min	Typ	Max
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	1.90	2.00	2.10
D2	1.40	1.50	1.60
E	2.90	3.00	3.10
E2	1.50	1.60	1.70
e	0.50BSC		
L	0.30	0.40	0.50
c	0.10	0.15	0.20
Nd	1.50BSC		

Note：1. Dimensions are not to scale

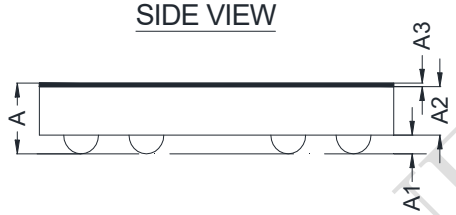
	TITLE	DRAWING NO.	REV
PUYA	Puya DFN8L 2x3X0.5-0.5PITCH POD	QRPD-0023	1.0

7.4 WLCSP8



COMMON DIMENSIONS
(Unit of Measure =mm)

SYMBOL	MIN	TYP	MAX	NOTE
A	0.530	0.565	0.600	
A1	0.170	0.190	0.210	
A2	0.320	0.350	0.380	
A3	-	0.025	-	
D	2.770	2.800	2.830	
E	1.765	1.794	1.825	
e	-	1.000	-	
e1	-	1.200	-	
e2	-	2.100	-	
F	0.397REF			
J	-	0.200	-	
G	-	0.500	-	
H	0.350REF			
K	0.197REF			
b	0.245	0.270	0.295	



PIN ASSIGNMENT MATRIX

	A	B	C	D
1	-	-	SCL	-
2	Vcc	WCB	-	SDA
3	NC	-	-	Vss
4	-	NC	E2	-

NOTE: 1.Dimensions are NOT to scale.
2.Solder ball composition is SnAg.
3.Product offered with Back Side Coating(BSC)

	TITLE	DRAWING NO.	REV
PUYA	8-ball,1mm pitch Wafer Level Chip ScalePackage	CS-8	A

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand

Order quantity needs to be multiple of the minimum quantity

8. Revision History

Version	Content	Date
Rev 1.0	Initial Release	2020-10-28
Rev 1.1	Update Pin Definition Item 6, 7	2021-03-26
Rev 1.2	Update feature, Item3 DC Characteristics	2021-05-01
Rev 1.3	1) Add package of 'SOP8,TSSOP8 and UDFN8' 2) Add Device Power up/Power down description	2021-12-01
Rev 1.4	1) Update 'Package information' 2) Update reliability parameters	2022-02-03
Rev 1.5	Update "Table3-1"	2023-01-18
Rev 1.6	1) Add 105C, Update Isb 2) Update Ordering Code Detail	2023-02-20
Rev 1.7	Updata page write lower address bit length	2024-05-08

Puya Semiconductor Co., Ltd.